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APPLICATIONS

RIE-induced carrier lifetime degradation

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ABSTRACT

Reactive Ion Etching (RIE) is used in the fabrication of some types of solar cells to achieve a highly directional etch. However, cells fabricated using RIE have lower than expected efficiency, possibly caused by increased carrier recombination. Characterisation of the carrier lifetime in solar cells was conducted using the quasi steady state photoconductance (QSSPC) measurement technique. Substantial effective lifetime degradation was observed for silicon samples processed by RIE. Lifetime degradation for samples where RIE etches into silicon is found to be permanent, while for samples where RIE etches only on dielectric layers of SiO_2 grown on the wafer, the lifetime degradation is found to be reversible. The reversible degradation in RIE-processed samples is associated with radiation damage. By reducing the proportion of a wafer exposed to RIE, the degradation of the effective lifetime of RIE-etched silicon samples can be minimised, and the performance of silicon solar cells can be improved significantly. Copyright © 2010 John Wiley & Sons, Ltd.

KEYWORDS

RIE; carrier lifetime; QSSPC; radiation damage

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1. INTRODUCTION

Reactive Ion Etching (RIE) is used in the fabrication of some types of speciality silicon solar cells because it provides a highly anisotropic etch profile with good etch-mask selectivity, is suitable for complicated etch patterns and is free from dangerous wet chemicals [1–3]. It has been extensively used in fabrication of nanopores in silicon [4], memory devices [5], multilevel interconnect Si devices [6], photonic crystals [7,8] and microelectromechanical systems [9].

Though the use of RIE is not widespread in the photovoltaic (PV) industry, the benefits of RIE have started to be recognised. Nositschka used RIE to texture multicrystalline silicon solar cells for lowering of reflectance [10]. Agostinelli studied the benefit of dry etching for integration to obtain improved performance and lower environmental impact [11,12]. However, RIE generates defects in the near-surface region of the semiconductor [13–15], thus degrading the electrical performance of solar cells and other devices [16–19]. Deenapanray characterised the reaction mechanism of RIE etching of silicon, SiO_2 and SiN_x against varied etch parameters [20,21], and also studied lifetime degradation and defect characterisation in RIE-processed silicon samples [22]. SLIVER technology developed by Blakers and Weber enables the production of 20% efficient cells by incorporating the benefits of RIE [23,24].

The very high efficiency solar cell (VHESC) program sponsored by DARPA adopts the six-junction independently-wired tandem cell approach [25,26]. Most of the light incident on the cell package is filtered by high-band gap solar cells and light in the wavelength range from 875 to 1100 nm will only fall onto silicon. The role of the silicon cell is to convert 7% of the light incident on the tandem structure into electricity.

Development of the silicon VHESC solar cell comprises complex fabrication steps to be performed on very small silicon solar cells ($2.5 \times 8\,mm^2$), and the use of RIE offers the option to replace many conventional wet chemical etching steps, thus shortening the number of processing steps and also increasing the yield. In this paper we investigate carrier lifetime degradation associated with RIE processing, and methods to reverse some types of this degradation.

2. EXPERIMENTAL

RIE was performed in an Oxford PlasmaLab80 system using CHF_3 plasma with the addition of O_2. The process

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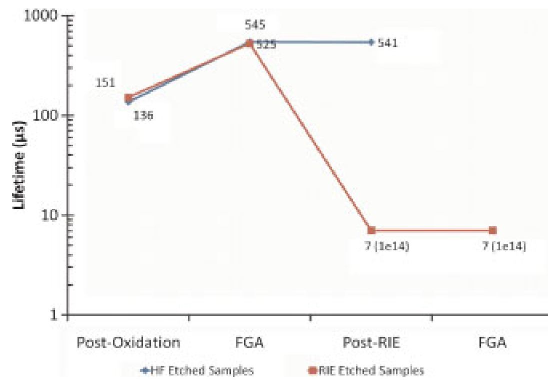

Figure 1. Before and after etching of silicon samples by wet chemical and RIE. The figures in brackets refer to the injection level during PCD measurement.

pressure was 55 mTorr and the total gas flow rate was kept constant at 55 SCCM (cubic centimetre per minute at STP). Samples were placed on the water-cooled (25°C) bottom electrode that was powered by a 13.56 MHz RF generator. The parallel upper and lower electrodes are 240 mm in diameter. The RF powers reported are forward powers, as the measured reflected power was insignificant. The etch speeds of thermally grown SiO_2 were measured to be 18 and 44 nm/min at an RF power of 100 and 200 W, respectively.

P-type float zone <100> 100 mm diameter high resistivity silicon wafers were used in the experiments. They were etch-polished, cleaved into quarter-piece samples, cleaned and thermally oxidised to a thickness of 120 nm, followed by forming gas annealing (FGA) in 10% hydrogen in nitrogen at 400°C for 30 min. Effective carrier lifetime was measured at an injection level of 10^{14}–10^{15} carriers per cm^3 using photoconductance decay (PCD) [27,28]. Effective carrier lifetime represents bulk and surface recombination. In the interests of experimental simplicity and clarity, no surface phosphorus diffusion (to suppress surface recombination) was used.

3. RESULTS AND DISUCSSION

3.1. Wet and dry etching (RIE) of silicon wafers

Samples were oxidised and annealed in forming gas as described above. The oxide on some samples was then etch-removed in hydrofluoric acid (HF), while the oxide on other samples was etched in 200 W RIE plasma for 3 min. The RIE etch process time (3 min) was sufficient to remove all of the oxide and to etch a fraction of a micron of silicon. After the etching, all samples were re-passivated by thermal oxidation, and then effective carrier lifetime was measured, as shown in Figure 1 for typical samples. Substantial lifetime degradation was observed for post-RIE etched samples as compared to HF etched samples.

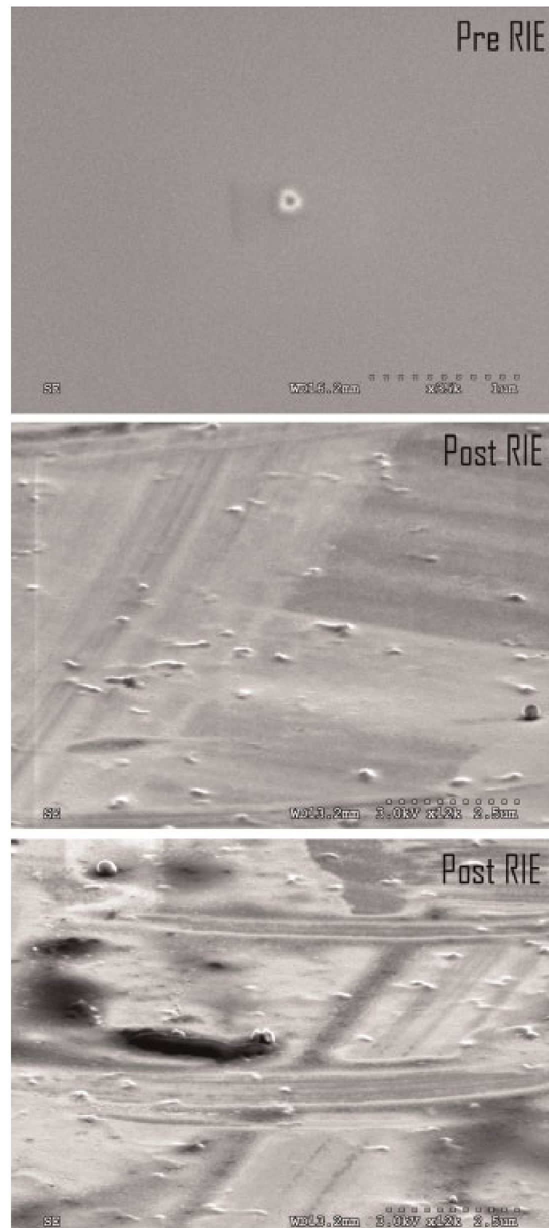

Figure 2. SEM pictures for samples before and after being processed by RIE.

This lifetime could not be recovered by a subsequent forming gas anneal. Figure 2 shows SEM pictures for samples before and after RIE etch. Post-RIE samples were associated with surface damages caused by ion bombardment.

The passivation oxide of these RIE samples was stripped, and silicon was then etched in tetramethyl ammonium hydroxide $(CH_3)_4NOH$) (TMAH) for varying times for different samples. After etching in TMAH, the samples were re-passivated with oxide followed by annealing in forming gas. The effective lifetime was measured as shown in Figure 3. The aim of this work was to

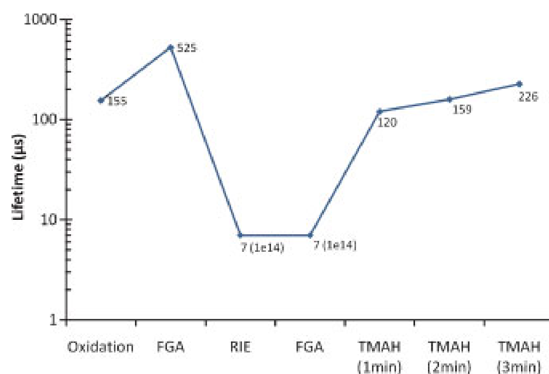

Figure 3. Improved recovery of sample lifetime after etching in TMAH for longer periods of time.

understand whether the RIE-induced damage is shallow or deep within the silicon. Improved recovery of carrier lifetime was observed for samples that were TMAH etched for longer times. The fractional recovery of sample lifetime by etching in TMAH for 3 min is approximately 40%. Complete recovery of lifetime (~525 µs) can be achieved by etching in TMAH for 10 min, which corresponds to an etch-depth of about 10 µm.

3.2. RIE etching of oxide layers

The effect of an RIE etch of thermal oxide on silicon, when the etch is sufficiently short to avoid penetration of the oxide, was investigated. The results for a variety of powers and times are shown in Figure 4. Lifetime degradation was observed for all samples, although the degradation was considerably less than in the case where the RIE etch penetrates the oxide into the silicon.

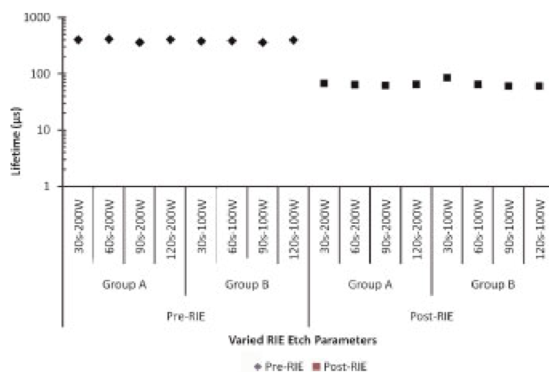

Figure 4. RIE etching of oxide only without penetrating into silicon. Samples in group A were processed with 200 W RF power while group B was processed with 100 W RF. The varying etch time for both groups of samples was performed at 30s, 60s, 90s and 120s.

Post-RIE lifetime degraded samples were then cleaned in isopropanol solution to remove any unwanted surface charge built up from RIE and lifetime was remeasured. Lifetime degradation showed no sign of improvement.

Samples were then etched in HF solution to remove a few nanometre of the oxide layer, to investigate whether the RIE damage was located near the surface. However, there was no improvement in lifetime. These two results suggested that surface effects were not causing the lifetime degradation.

It was found that the lifetime of the degraded samples could be recovered by annealing [29]. Group A samples were subjected to Rapid Thermal Annealing (RTA) at 400°C in the presence of nitrogen for 3 min. Group B samples were thermal annealed at 400°C for 30 min in nitrogen. As shown in Figures 5 and 6, complete restoration of lifetime resulted in each case.

The phenomenon of effective carrier lifetime recovery could be related to radiation damage. References have shown that radiation induced by plasmas generates trapping sites in oxide layers when exposed to RIE [30]. So long as the RIE etch does not penetrate into the silicon, the loss of the lifetime can be recovered by annealing in nitrogen.

RTA in nitrogen ambient was used in addition to thermal annealing in nitrogen environment since RTA is an enclosed system with no possibility of hydrogen being introduced during the annealing process, thus ruling out the possibility of carrier lifetime recovery due to potential hydrogen introduction. In terms of the lifetime recovery, there is no difference observed between RTA annealing and thermal annealing in a nitrogen environment.

3.3. Lifetime degradation from fractional RIE exposure

The work described above demonstrates that the degradation of lifetime resulting from RIE etching of the silicon surface can be partially recovered by wet chemical etching of the silicon surface after RIE. However, this would generally be inconvenient, since it is an additional step and could negate some of the benefits of RIE such as etch anisotropy.

In many process sequences, only a small portion of a wafer surface will be exposed to RIE. It would not be surprising if the degree of carrier lifetime degradation in the wafer was dependent upon the fraction of the surface area exposed to the etch process. The effect of fractional exposure to RIE etching was investigated with the aid of shadow masks with varying fractional apertures, as shown in Figure 7. The fractional exposure is calculated as the area of windows divided by the mask's surface area.

P-type float zone <100> 100 mm diameter high resistivity wafers were first cleaved into quarter-sized samples, oxidised and annealed in a forming gas environment at 400°C for 30 min, followed by RIE etching and FGA anneal. Carrier lifetime of these samples was

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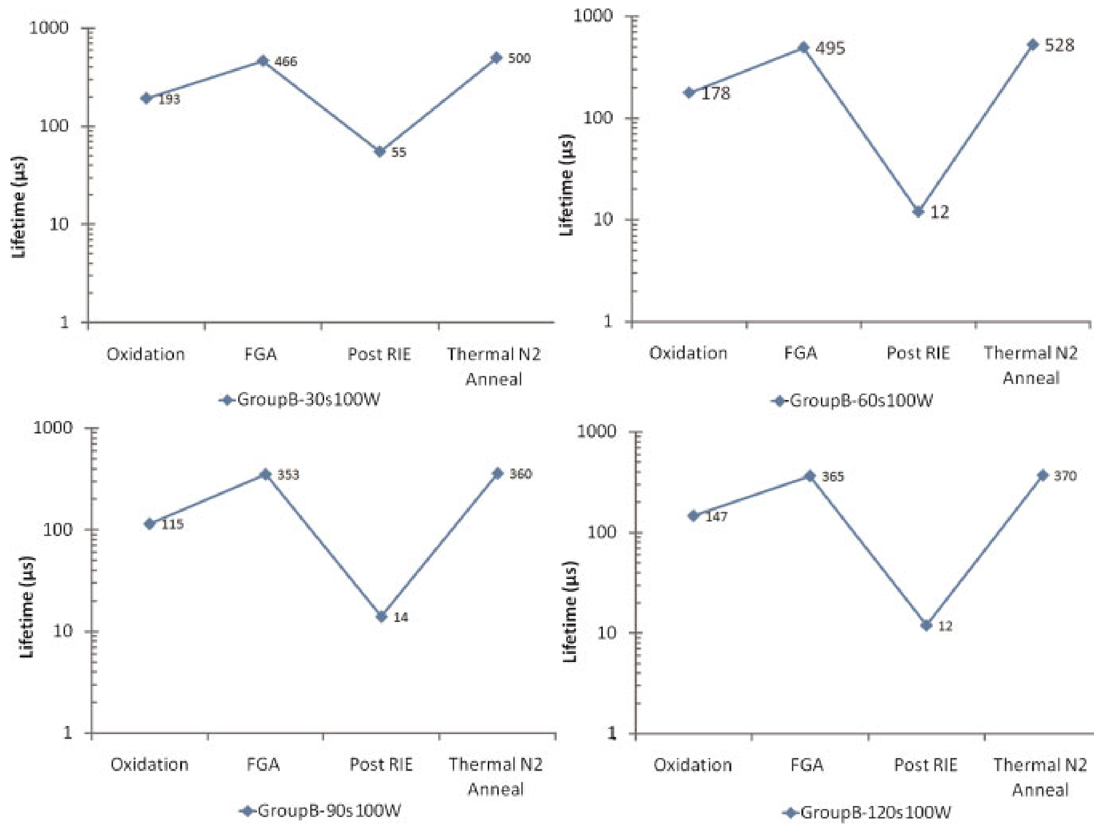

Figure 5. RIE etched samples (Group B) after thermal treatment at 400° for 30 min.

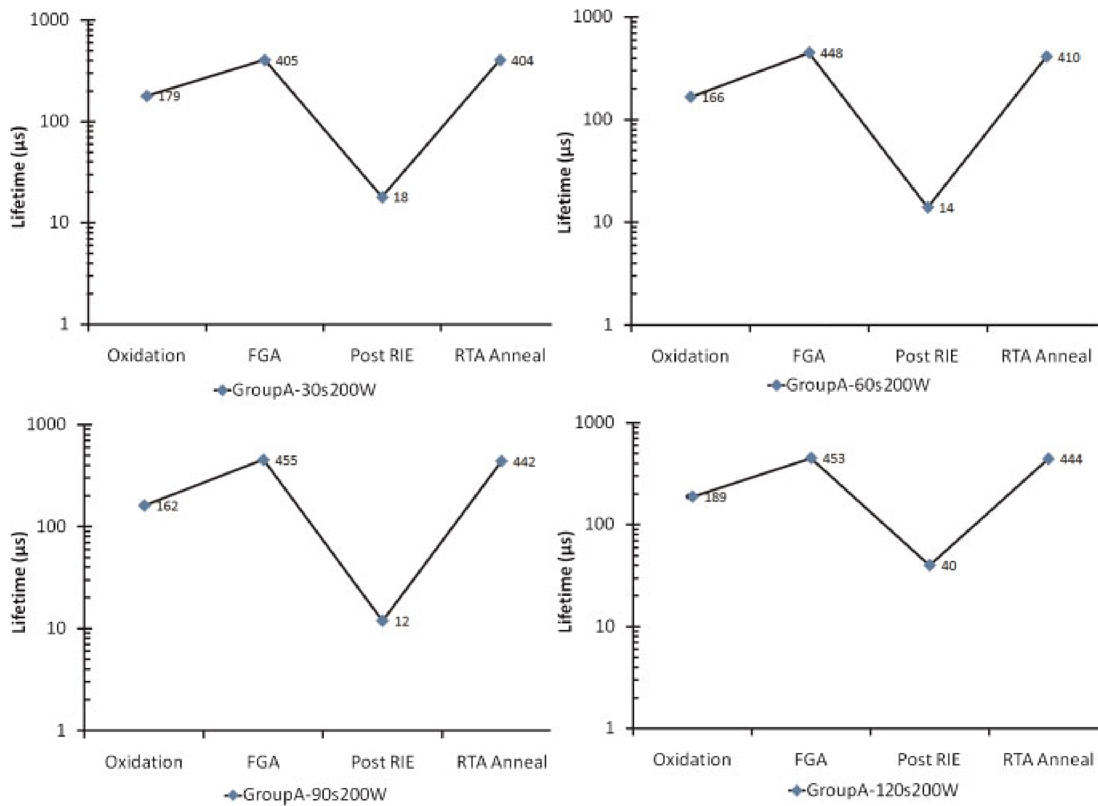

Figure 6. RIE etched samples (Group A) after rapid thermal anneal at 400° for 3 min.

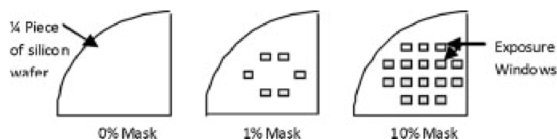

Figure 7. Masks (a quarter size of 100 mm wafer) with varied degree of exposure windows to RIE.

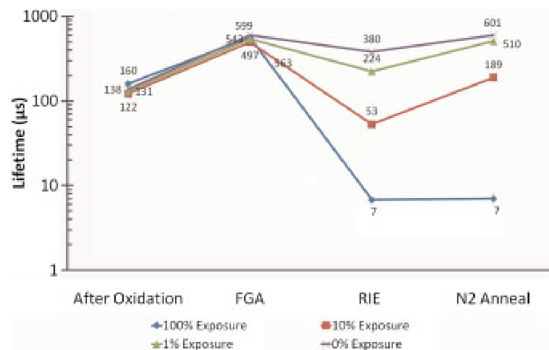

Figure 8. SiO_2 grown samples processed by varied degree exposure to RIE for 7 min.

measured and recorded following each step. The PCD method uses a large coil to detect average excess carrier concentrations beneath the coil surface. This approximates the situation in a device such as a solar cell, whereby parameters such as open circuit voltage depend upon some form of areal average carrier lifetime.

Half of the samples were exposed to RIE for 3 min and half for 7 min, using RF power of 200 W while maintaining the rest of etch parameters constant. During RIE, the samples were covered by masks that have 0, 1, 10 and 100% exposure windows. Based on RIE etch rates, the 3 min etch will etch through the oxide plus a small fraction of a micron of silicon, while the 7 min etch will etch about 0.3 µm of silicon. After RIE, samples were annealed in N_2 at 400°C for 30 min. Typical carrier lifetime measurements are shown in Figure 8 for the 7 min etch. The 3 min etch produced similar results.

Results show that samples processed with 100% of RIE exposure suffer permanent carrier lifetime degradation. Samples exposed to 10% of RIE processing suffer reduced, but still substantial, carrier lifetime degradation. However, the damage can be partially repaired by annealing. Samples that received 0 and 1% of exposure to RIE suffered modest lifetime degradation that could be fully repaired by annealing.

Figure 9 depicts fractional carrier lifetime degradation as a function of fractional exposure to the RIE. The degradation in the measured carrier lifetime is approximately logarithmically dependent upon the exposure fraction.

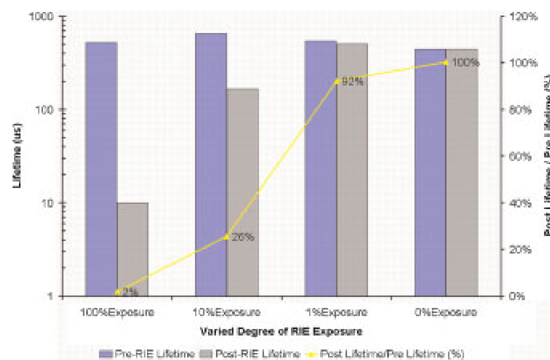

Figure 9. Post-annealing carrier lifetime in samples etched with RIE for 7 min.

4. CONCLUSION

Severe carrier lifetime degradation was observed in oxidised silicon wafers subjected to RIE etching, regardless of whether or not the etch process penetrated the oxide.

If the etch did not penetrate the oxide then the carrier lifetime could be fully recovered by a 400°C anneal in nitrogen. This is consistent with radiation damage being the cause. RIE can be used to open windows in a dielectric such as SiO_2. Provided the RIE etch is terminated before reaching the silicon, then any degradation in carrier lifetime is fully recoverable by annealing. Completion of removal of the dielectric could be through use of a non-damaging process such as wet etching.

If the RIE etch penetrated the oxide and commenced to etch the silicon then lifetime could not be recovered by a subsequent anneal. However, the degree of observed lifetime degradation was approximately logarithmically dependent upon the fraction of the wafer surface exposed to the etch, through use of a shadow mask. When the exposure fraction is 1% or less, the degree of degradation was observed to be minimal. RIE can be used to open small windows (for example, for an electrical contact) in a dielectric by etching through into the silicon. Etching into the silicon avoids the need to remove residual dielectric using a wet etch. The carrier lifetime will be minimally affected provided that the window area is a few per cent or less.

Cells fabricated by incorporating dry etching (RIE) can achieve high performance provided that carrier lifetime degradation induced by RIE be circumvented, either by confining the etching to a surface passivation oxide dielectric, or by limiting the exposure to RIE to a small fraction of the surface if penetration of etch into silicon is unavoidable.

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