Miniature Silicon Solar Cells for High Efficiency Tandem Cells

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Abstract— **In this paper, a discussion is made of the design of silicon cells to be used in a six-junction tandem solar cell structure as part of the Very High Efficiency Solar Cell (VHESC) program. Minority carrier recombination at surfaces and in the volume, internal quantum efficiency, resistance losses, free carrier parasitic absorption, optical reflection, light trapping, and light absorption must be traded off against each other. Modelling was used to analyse the various parameters and produce estimates of short circuit current, fill factor and open-circuit voltage of the cell. In addition, quasi-steady-state phtotoconductance measurements to analyse carrier recombination and emitter saturation current (Joe) as well as to predict the open-circuit voltage of solar cell is presented. For metallisation of such small solar cells, alternate methods of making contact such as light-induced plating and electrolyte plating in addition to evaporating metal on the contacts were explored and employed. Numerical resistive loss modelling was made to calculate the optimum metal thickness achieved by light-induced and electroplating to minimise resistive losses. Experiments were conducted to determine the proper plating rate by light-induced and electrolyte plating. Cells were fabricated by standard silicon processing techniques followed by testing of IV curves using current-voltage flash-tester to achieve the target efficiency.**

Keywords-PC1D, QSSPC, Light-Induced Plating, RIE.

I. INTRODUCTION

A major objective for photovoltaic conversion is to develop high efficiency solar cells. Researchers at ANU have been conducting research on miniature silicon solar cells to be used in conjunction with six-junction tandem solar cells. In six-junction tandem solar cell as shown in fig 1.1, individual solar cells will be arranged so that each solar cell absorbs the appropriate slice of the solar spectrum. The eventual goal of six-junction tandem solar cell package is to achieve the combined efficiency of >50% under 20suns illumination. Silicon is one of the cells in the tandem structure, and absorbs energy of 1.42 – 1.1 eV. The role of the silicon cell is to convert 7% of the light incident on the tandem structure into electricity. Other cells in the stack contribute the balance of the electricity. Key design parameters for the silicon cells are that it should have dimensions of 2.5×8 mm^2 and it needs to transfer light energy of less than 1.1eV to the underlying solar cells.
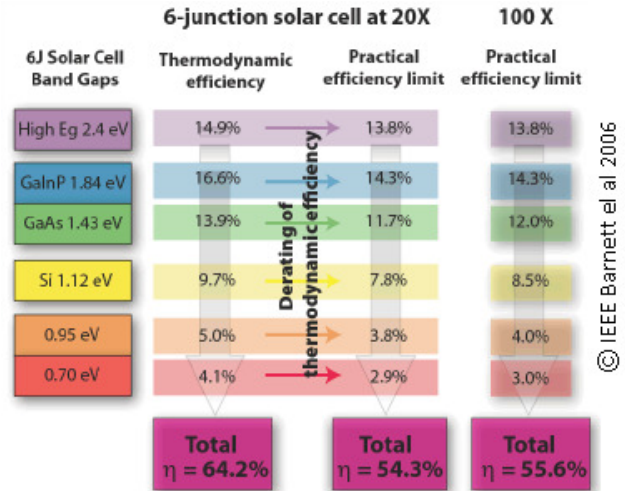

Fig 1.1 Band Gap for Six-Junction Tandem Stack

II. CELL STRUCTURE AND DESIGN

The external dimensions of the silicon solar cell have to be 2.5mm in width and 8mm in length. Cells were fabricated using 450μm thick <100> p-type float-zone 1Ωcm wafers. The cells have an active n-type emitter region on both front and back of cell with the dimension of 6.5×2.5 mm^2. Metal contacts are made to both sides of the cell. The n-contact to the external world is on sunward side and the P-contact is on the back of cell. Metal contacts are designed with a spacing of 1.9mm in the lateral direction and 5.5 mm in the lengthwise direction as shown in the figure 1. Multiple cells are processed simultaneously on each wafer until the metallization step is completed, at which time they are diced out of the wafer to form individual solar cells.
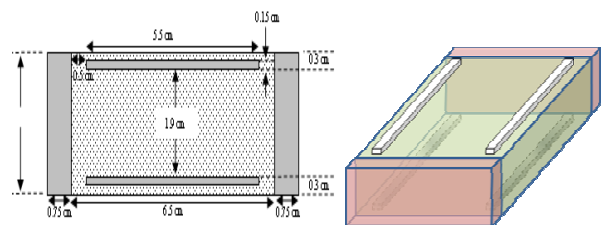

Fig.2.1 Top view and 3D view of Silicon solar cell

1.1 Illumination

Sunlight with power of 2W/cm^2 (20 suns) is incident on the top of the package. GaAs and other high bandgap cells will absorb much of this light. Light of energy <1.42eV (875nm) will be transferred to the Si cell. Light of energy E<1.1eV must be transferred with high efficiency to underlying cells. Therefore, BSR and texturing cannot be used. A polished cell will have to be thick, 0.5-2mm, to have a reasonable efficiency of conversion in the weak-absorption wavelength range 875-1100nm.

1.2 Recombination at Surface, Edges and Contacts

The cells have a combined surface area (front, back and sides) of about 50 mm^2 A reasonably good surface passivation can be grown using thermal oxidation to minimize surface recombination. Edge recombination in small cells is a formidable problem. Since the cells are small, they need to be processed in a host wafer, for practical reasons. Hence, cells will be cut out of the host wafer before the final oxidation to allow oxide passivation to minimize recombination at the cut/scribed edge. Contact recombination will be suppressed with small contacts (~1%) and/or heavy doping beneath the contacts.

1.3 Anti-Reflective Coating

The cells will be surrounded by an optically thick n=1.4 medium. Oxide and nitride coating thickness of 30nm and 90nm respectively gives rise to a loss of 1% and 3% in air and under encapsulation, and is reasonably close to optimum for both. The oxide coating is required to prevent damage caused by direct deposition of LPCVD nitride on silicon.

1.4 Internal Quantum Efficiency

To achieve IQE above 99%, the diffusion length will be kept above 3-4 times the cell thickness. Bifacial cells can be roughly twice as thick for the same IQE because they have a junction on both surfaces.

1.5 Resistive Losses

For a 50μm, 100μm and 500μm thick polished cell, 65%, 74% and 87% of the 875-1100nm light will be absorbed in the top half of the cell respectively. For a 100μm thick textured cell, 64% of the light will be absorbed in the top half of the cell. Therefore current sharing in a cell with a junction on both surfaces is a significant but not overly important factor in reducing emitter resistive losses. Additionally, the electron current in the rear phosphorous diffused layer of a bifacial cell will be small, and so will resistive losses.

1.6 Lateral Diffusive Losses

Electron and hole currents can be extracted from the two edges or the two ends or both. The sheet resistance of a 500 micron thick, 1 ohm-cm wafer is 20 ohms/sq, which is much lower than the phosphorus diffusion sheet resistance. Therefore electron resistive losses are of more concern than hole resistive losses.

The best arrangement is to have n-contacts at both edges and both ends of the active area. These will be on top because most of the current is generated close to the top surface. The p-contacts will be on the bottom, near both edges and optionally on both ends as well. Based on calculation, estimated resistive loss will be less than 5%.

III. PC1D MODELLING FOR CURRENT-VOLTAGE AND IQE

PC1D modelling was used to predict the expected current and voltage as well as IQE of 2.5x6mm silicon solar cell. Major parameters used for modelling include active area of 15mm; one-sun intensity; bifacial emitter diffusion; and heavy n+ and p+ diffusions. Modelling was also done without GaAs being covered on top of silicon. Modelling predicts short-circuit current of around 4.17mA and open-circuit voltage of 630mV (fig 2.1).
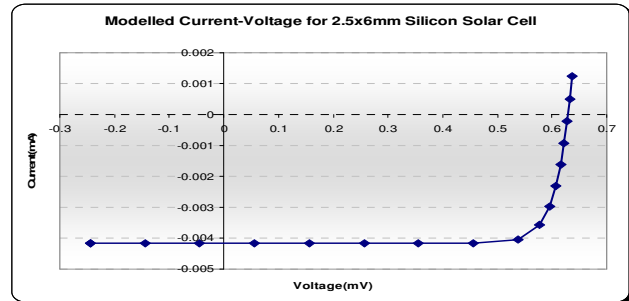

Fig 2.1 Modelling of Current-Voltage

Since light incident on silicon solar cell will be filtered by GaAs and other higher band-gap materials, most of the light silicon absorbs will be in the range of 800nm to 1100nm. Modelling also predicts that EQE of up to 90%can be achieved in the desired range (fig 2.2).
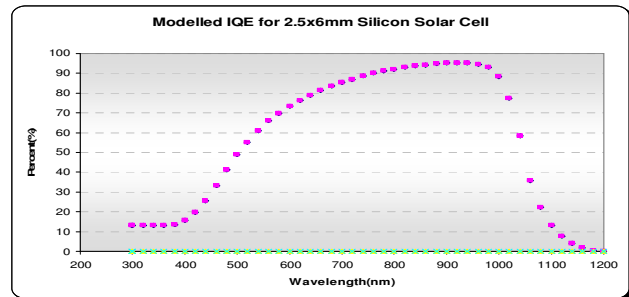

Fig 2.2 Modelling of Internal Quantum Efficiency

IV. CHARACTERISATION OF LIFETIME AND EMITTER SATURATION CURRENT DURING EACH PROCESS

Before the fabrication of the cells, characterisation of samples using QSSPC measurement technique [2, 3] was carried out to identify the behaviour of recombination mechanism including effective carrier lifetime (τ_{eff}) and emitter saturation current (J_{oe}) after each high temperature processing step.

3.1 Experiment

P-type float-zone, (100), 120Ω.cm resistivity, 450μm thick

wafers were etched in HF:HNO₃ solution to remove saw damage. Wafers were then cleaned in standard solutions to remove organic and inorganic contaminants. Emitter diffusion was performed at achieve the sheet resistance of 100 Ω/□ followed by the growing of a thin silicon dioxide layer to passivate the diffused layers. SiN_x was deposited to act as an anti-reflection layer. Heavy phosphorous diffusion was performed following the opening of small pockets in the anti-reflection layer. Oxidation was again performed after heavy phosphorous diffusion to grow a masking oxide which will act as a diffusion barrier against subsequent heavy boron diffusion. Heavy boron diffusion was following the opening of small pockets, before treating wafers in forming gas annealing environment to reintroduce the loss of hydrogen during the high temperature processes.

3.2 Characterisation by QSSPC Technique

Quasi steady state photoconductance (QSSPC) measurement was performed after each diffusion, oxidation and nitride deposition processing steps to analyse the effective carrier lifetime as well as emitter saturation current. Adequate effective carrier lifetime of around 560μs was maintained after the end of forming gas annealing as shown in fig 3.1. Using the implied-Voc technique [2], the final open-circuit voltage is predicted to be around 640mV. Emitter saturation current was also extracted from QSSPC data to analyse the surface recombination. Value of surface recombination was also maintained low at around 25 fA/cm^2 after the last forming gas annealing step as shown in fig 3.2.
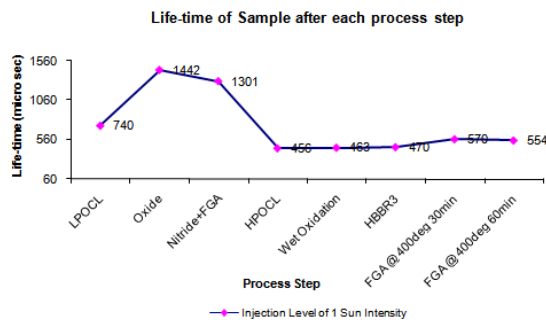

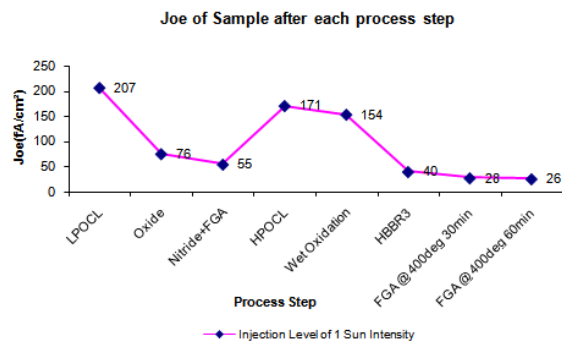Fig 3.1 Effective Carrier Lifetime after each Processing Step

Fig 3.2 Emitter Saturation Current after each Processing Step

V. CELL CONTACTS PLATING

Since the metal contacts to silicon solar cells are relatively small, if a technique of metal evaporation is used a selective metal mask will need to be machined highly accurately by a laser machining technique. In addition, to selectively evaporate metals on the contacts, alignment of the mask on the contact opening can be quite difficult, possibly resulting in metals being evaporated on the active area, causing shading losses and shunting. To address these issues, plating of metal contacts by light-induced plating and electrolyte plating are considered as preferred options .

4.1 Light-Induced Plating

The light-induced plating (LIP) technique was initially developed and patented in 1979 by Solarex [5]. The compelling advantage of LIP compared to conventional electroplating is by exploiting the photovoltaic effect of a solar cell, it is possible to utilize the advantage of the electrolytic plating solutions without the need to contact the front side metal grid. The solar cell itself generates the required current. The basic principle of light-induced plating is shown in figure 4.1. Light-induced plating has been employed frequently in high performance solar cells [6] and solar cells with large area contacts [7, 8]. In our research, Light-induced plating technique will be used for plating small area n++ contact of silicon solar cells with Ag.
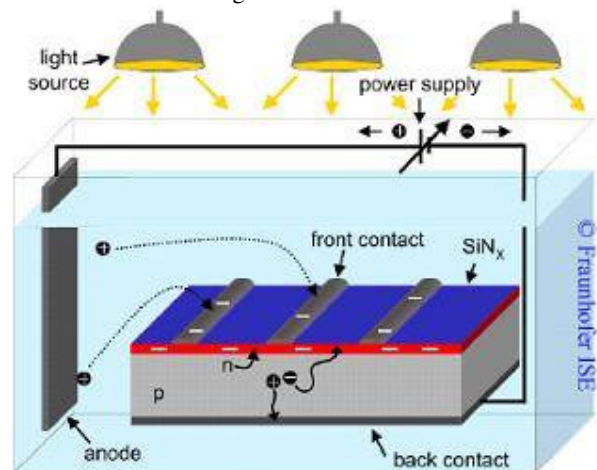

Fig 4.1 Principle of Light Induced Plating

4.2 Electrolyte Plating

Since light-induced plating technique is only suitable for plating front contact (n++) of silicon solar cell, a direct-contact electroplating method was chosen to plate back contact (p+). Electroplating is the process of using electrical current to reduce metal cations in a solution and coat a conductive object with a thin layer of metal. The benefit of above the plating set up (fig 4.1) is that it provides an option of employing both light-induced plating and electrolyte plating simultaneously for silicon solar cells contacts.

4.3 Experiments to Identify Rate of Light-Induced and Electrolyte Plating

P-type float zone, (100), 1000Ωcm, 450μm thick, double-sided polished wafers were firstly RCA cleaned. Then an LPCVD nitride with thickness of around 40nmwas grown. Small openings were made and an emitter phosphorous diffusion on front side of wafer was performed. Diffusion was performed to achieve sheet resistance of $5\Omega/\square$. The rest of the wafer surface with nitride acts as a diffusion barrier. The back side of wafer was then etched to make openings for boron contact. After RIE, the wafer was dipped in 10% HF to remove any native oxide and nitride remaining on phosphorous and boron diffusion openings. Both sides of wafer were evaporated with Cr/Pd to a thickness of around 40nm and forming gas annealed at 400'C for 30mins to make good ohmic contact. The wafers were then subjected to light induced plating and electrolyte plating to further thicken the metal contacts as shown in figure 4.1. After the plating, plated Ag metal thickness was measured in Atomic Force Microscopy to determine the growth rate. Measurement data from AFM are plotted and figure 11 has shown that average Ag growth rates by light-induced plating are approximately 1.04um/min at 160V for 3mins and 0.98um/min at 120V for 5mins; and by electrolyte plating are 9.8um/min at 0.1A, 0.08V for 3mins and 0.97um/min at 0.05A, 0.03V for 5mins.
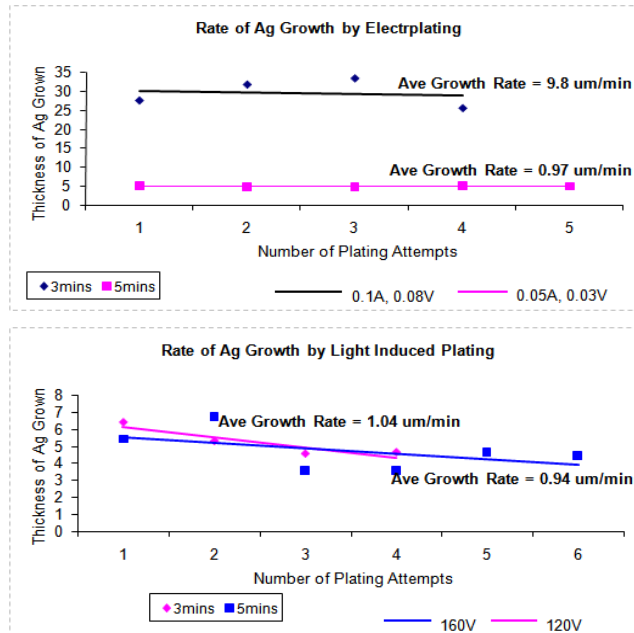

Fig 4.2. Measurement of Ag Growth Rate by Electrolyte and Light-Induced Plating

Thickness of Ag on both phosphorous and boron contacts are also measured using optical microscope (figure 4.3) and results obtained are observed comparable to AFM.

4.3 Numerical Resistive Loss Modelling

Numerical modelling is made to calculate the required Ag metal thickness to ensure that total resistive loss for four silver contact bars is below 0.1% of total power output. Estimated maximum power output for a cell with a dimension of 0.55cm and 0.2cm under 1 sun intensity, P_{max} = 1.98mW.
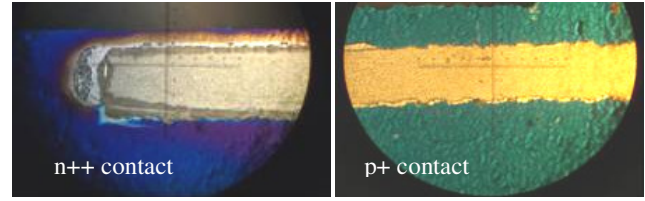

Fig 4.3. Optical Microscope Measurement on Plated Cells

For a silver bus bar with a width of 0.02cm; length of 0.55cm; considering the half of current generated by light in the emitter has entered equally into each silver bus bar; and assuming the worst case scenario of current (generated by illumination) entering from one end of silver and extracted from the other end of silver, power loss per each silver bar can be calculated by equation 1 and power loss by percentage of each silver bar by equation 2.

$$P_{loss\,Silver} = 2I^2 R_{Silver} = 2I^2 \rho_{silver} \frac{l}{A} \qquad (1)$$

$$P_{loss\,Silver}(\%) = \frac{P_{loss\,Silver}}{P_{max}} x100\% \qquad (2)$$

Using the equations 1 and 2, power loss per silver bar can be calculated with respect to the varied thickness of Ag, as shown in table 1.

Table 1. Power Loss in Percentage by Silver Bar

	1μm thick Ag	5μm thick Ag
P_{loss} (%) / SilverBar	0.11%	0.02%
P_{loss} (%) / 4 SilverBars	0.44%	0.09%

VI.   FABRICATION AND TESTING

Cells were fabricated using standard silicon process techniques, as shown in the table 2. First batch of cells fabricated were having single-sided emitter only.

Table 2. Fabrication Sequence for Silicon Solar Cell

Step	Detail
Si Etch	Etch in HF:HNO
Laser Scribe	Form individual cells in host wafer
TMAH etch	Repair laser damage
RCA Clean	Clean organic/inorganic contaminants
LPCVD	Deposit nitride as a diffusion barrier
Open windows	Form emitter diffusion region
P Diffusion	Form active emitter region
Oxidation	Grow passivation oxide and drive-in
LPCVD	Deposit SiN Anti-reflection coating
Open windows	Make opening for n++ diffusion
P Diffusion	n++ diffusion

Oxidation	Thick oxide as a boron diffusion barrier
Open windows	Make p+ diffusion opening
Diffusion	p+ diffusion
FGA	Reintroducing the hydrogen
Metallisation	Form thin metal contacts to diffusion
Sintering	Form good ohmic contact
Plating	Thicken deposited metal
Sintering	Form good ohmic contact
Dicing	Cut individual cells out of host wafer
Testing	Test under 1 sun-illumination

Completed cells were diced out from wafer to form individual cell. After dicing, individual cells were wired with electrodes on both sides of n and p regions. Cells were tested by current-voltage flash tester [9] under 1 sun illumination intensity without having the light being filtered by GaAs. Cells tested were observed to have high shunt resistance but with slight series resistance and low open-circuit voltage, as shown in figure 5.1. Series resistance is caused by inadequate ohmic contact formed between the metal and diffusion but can be resolved by sintering process. Low open-circuit voltage was primarily caused by low minority carrier lifetimes due to processing problems that will be rectified in future devices. Recombination at the device edges was minimised by ensuring that the active emitter region was kept a distance of 1mm away from the cell edge that was diced out at the end of all processing steps to form individual cells before I-V testing,. In this way, open-circuit voltage loss due to edge recombination should be insignificant [10].
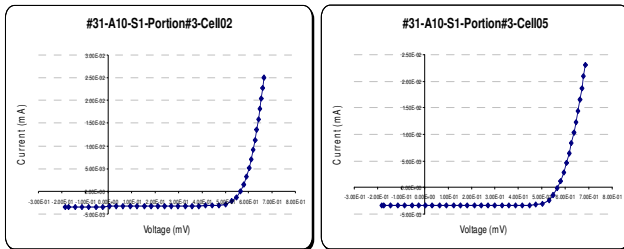

Fig 5.1 Current Voltage Tested under 1 Sun Illumination

Table 3 illustrates the values of open circuit voltage, short circuit current and fill factor of the cells tested without having the spectral filter (eg. Using a GaAs cell).

Table 3 IV Data for Cell Tested up to 2 Suns Illumination

Intensity	Voc(mV)	Isc(mA)	FF (%)
Cell01	565	3.4	70
Cell02	566	3.36	75
Cell03	569	3.38	79

VII. CHARACTERISATION OF LIFETIME AND IMPLIED-V_{OC}

QSSPC measurement technique [2, 3] was again used to characterise the recombination that can be associated with the fabricated silicon solar cell.

6.1 Experiment 1

P-type float zone, (100), 120Ωcm, 450µm thick wafers were used for the characterization. Wafers were split into two groups and processed as shown in the table 4. Nitride and Oxide were deposited on two different groups of wafer initially to replicate the step of diffusion mask in fabrication solar cells.

Table 4. Characterisation Steps for Recombination

	1st Group of Wafer	2nd Group of Wafer
1	Deposit Nitride	Grow Oxide
2	Measure Lifetime	Measure Lifetime
3	Strip Nitride in HF	Strip Oxide in HF
4	Diffusion	Diffusion
5	Grow Oxide	Grow Oxide
6	Grow Nitride	Grow Nitride
7	Measure Lifetime	Measure Lifetime

Measured lifetime data has shown that samples using nitride directly deposited in silicon as a diffusion mask have much lower lifetime (<300µs) than samples using oxide as a diffusion mask (fig 6.1).
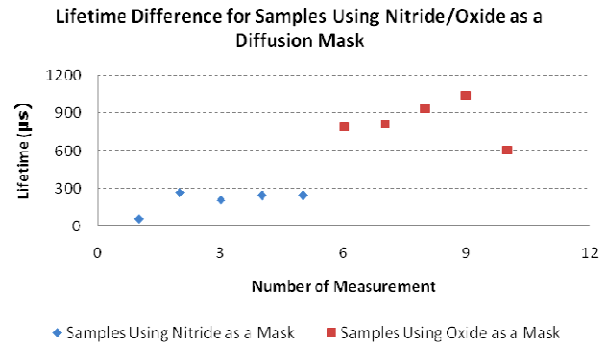

Fig 6.1 Lifetime for Samples Using Oxide/Nitride as a Mask

Similarly implied-Voc for samples using nitride as a mask were lower than that of oxide samples as shown in fig 6.2. Based on that, it has seen that depositing nitride directly on the silicon to be used as a diffusion mask can result in lower lifetime and open-circuit voltage.
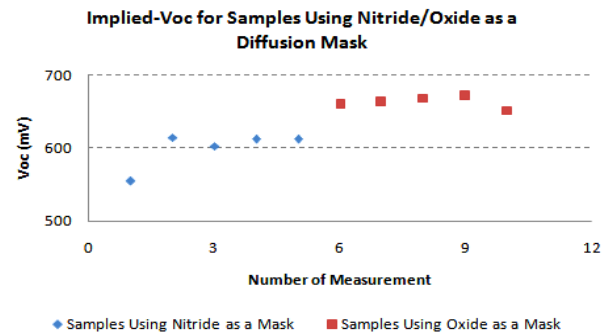

Fig 6.2 Voc for Samples Using Oxide/Nitride as a Mask

6.2 Experiment 2

Experiment was further conducted to see if using dry etching, RIE has any impact on carrier lifetime. P-type float zone, (100), 120Ωcm, 450μm thick wafers were again used for the characterization. Sample was oxidised and effective carrier lifetime was measured followed by etching oxide by RIE. Sample wafer was then cleaved into 4 pieces of quarter wafer and diffusion was performed. Subsequently a passivation oxide and anti-reflection coating were redeposited. Finally lifetime was measured to compare against the lifetime of former samples using oxide and nitride as diffusion barrier.
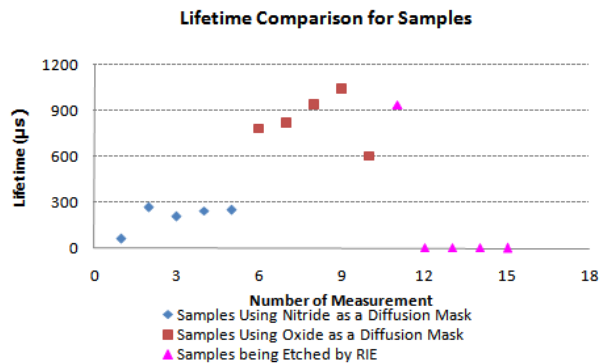

Fig 6.3. Lifetime for Samples Coated with Oxide/Nitride and Etched by RIE
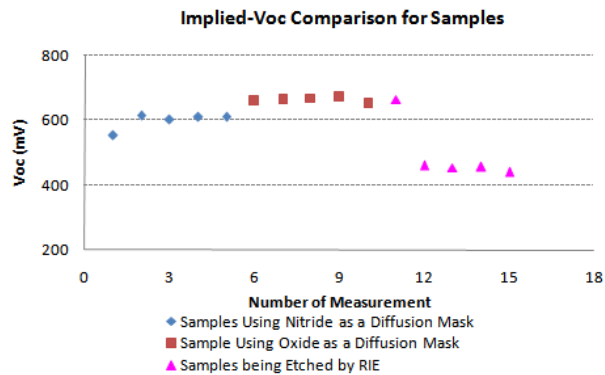

Fig 6.4. Implied-Voc for Samples Coated with Oxide/Nitride and Etched by RIE

As shown in fig 6.3, samples etched by RIE have resulted in significantly lower lifetime compared to any other samples and this could be due to damage induced by RIE [11, 12]. Implied-Voc extracted from the measured lifetime has also revealed that resultant Voc of RIE Etched samples are much lower (<550mV) than any other samples, as shown in fig 6.4.

VIII. CONCLUSION

The first batch of cells has been completed. They demonstrate the absence of shunts and a good fill factor. However, the open circuit voltage and current are low compared with the results expected from modelling due to process issues that will be rectified in future batches.

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