Design, Characterization and Fabrication of Silicon Solar Cells for >50% Efficient 6-junction Tandem Solar Cells

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***Abstract*—** A major objective for photovoltaic conversion is to develop high efficiency solar cells. Many approaches are under investigation – Multiple Junction Solar Cell, Multiple Spectrum Solar Cell, Multiple Absorption Path Solar Cell, Multiple Energy Solar Cell, and Multiple Temperature Solar Cells [1]. The Multiple Junction Solar Cell approach based on a six-junction tandem solar cell has been adopted to achieve conversion efficiency of greater than 50% in the VHESC program sponsored by DARPA [2]. In six-junction tandem solar cells, individual solar cells are stacked on one another and each solar cell absorbs the best-matched slice of the solar spectrum. Silicon is one of the cells in the tandem stacks, and absorbs photon energy of 1.42 – 1.1 eV. The role of the silicon cell is to convert 7% of the light incident on the tandem stack into electricity. Other cells in the stack contribute the balance of the electricity. Key design parameters for the silicon cells are that it should have dimensions of 2.5 x 8 mm^2 and it needs to transfer light with energy of less than 1.1ev to the underlying solar cells.

In this paper, discussion is made of the design of the silicon cell. Minority carrier recombination at surfaces and in the volume, internal quantum efficiency, resistance losses, free carrier parasitic absorption, optical reflection, light trapping, and light absorption must be traded off against each other. PC1D modelling is used to analyse the various parameters and produce estimates of short circuit current, fill factor and open-circuit voltage of the cell [3]. In addition, characterization of solar cell by photoconductance measurement to analyse carrier recombination and emitter saturation current as well as to predict the open-circuit voltage of solar cell [4, 5] is presented. Discussion of cell fabrication process followed by I-V testing is presented. Completed solar cells were tested in ANU using an in-house fabricated current-voltage flash tester [6] under AM1.5D.

I. Cell Sructure and Design

The external dimensions of the silicon solar cell have to be 2.5 mm in width and 8mm in length in order to fit the cell package. Cells were fabricated using 450µm thick <100> p-type float-zone 1Ωcm wafers. The cells have an active n-type emitter region on both front and back surfaces of the cell with the dimension of 6.5 x 1.9 mm^2. Metal contacts are made to both surfaces of the cell. The n-contact to the external world is on the sunward side and the p-contact is on the back of cell. Metal contacts are designed with a spacing of 1.9mm in the lateral direction and 6.5 mm in the lengthwise direction as shown in the figure 1. Multiple cells are processed simultaneously on each wafer until the metallization step is completed, at which time they are diced out of the wafer to form individual solar cells.

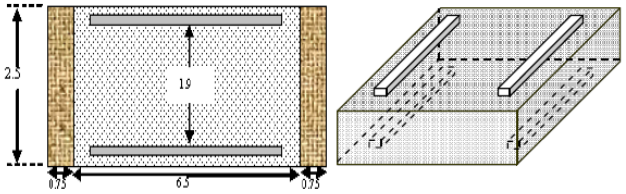

Fig.1 Top view and 3D view of Silicon solar cell

1.1 Illumination

Sunlight with power of 2W/cm^2 (20 suns) is incident on the top of the package. GaAs and other high bandgap cells will absorb much of this light. Light of energy <1.42eV (875nm) will be transferred to the Si cell. Light of energy <1.1eV must be transferred to underlying cells. Therefore, BSR and texturing cannot be used. A polished cell will have to be thick, 0.5-2mm, to have a reasonable efficiency of conversion in the weak-absorption wavelength range 875-1100nm.

1.2 AR Coating

The cells will be surrounded by an optically thick n=1.4 medium. Based on modeling calculations, oxide and nitride coating thickness of 30nm and 90nm respectively gives rise to a loss of 1% and 3% in air and under encapsulation, and is reasonably close to optimum for both.

1.3 Contact Recombination

Contact recombination will be suppressed with small contacts (~1%) and/or heavy doping beneath the contacts.

1.4 Surface Recombination

For a surface area of 50 mm^2 in total, a reasonably good surface passivation will be grown by using a thermal oxide.

1.5 Edge Recombination

Edge recombination in small cells is a formidable problem. Since the cells are small, they need to be processed in a host wafer, for practical reasons. However, it is highly desirable to cut the cell mostly out of the host wafer before the final oxidation to allow oxide passivation to minimize recombination at the cut/scribed edge.

1.6 IQE

To achieve IQE above 99%, the diffusion length will be kept above 3-4 times the cell thickness. Bifacial cells can be roughly twice as thick for the same IQE because they have a junction on both surfaces.

1.7 Resistive Losses

For a 50µm, 100µm and 500µm thick polished cell, 65%, 74% and 87% of the 875-1100nm light will be absorbed in the top half of the cell respectively. For a 100µm thick textured cell, 64% of the light will be absorbed in the top half of the cell. Therefore current sharing in a cell with a junction on both surfaces is a significant but not overly important factor in reducing emitter resistive losses. Additionally, the electron current in the rear phosphorous diffused layer of a bifacial cell will be small, and so will resistive losses.

1.8 Lateral Diffusive Losses

Electron and hole currents can be extracted from the two edges of the cell or the two ends or both. The sheet resistance of a 500 micron thick, 1 ohm-cm wafer is 20 ohms/sq, which is much lower than the phosphorus diffusion sheet resistance. Therefore electron resistive losses are of more concern than hole resistive losses.

The best arrangement is to have n-contacts at both edges and both ends of the active area. These must be on top because most of the current is generated close to the top surface. The p-contacts can be on the bottom, on both edges and optionally on both ends as well. Based on calculation, estimated resistive loss will be around 5%.

II. MODELING BY PC1D

PC1D modelling is used to analyse the short circuit current, open circuit voltage, fill factor and internal quantum efficiency under 1 sun illumination condition.

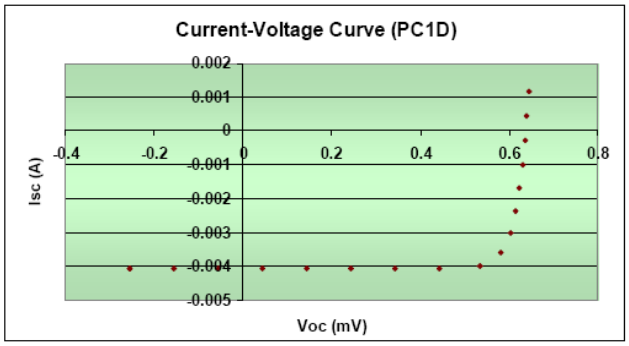

Fig.2 Current-Voltage curve by PC1D modelling

Modelling in fig. 2 estimates that short circuit current should be around 4.2mA while open circuit voltage should be around 630mV.

Internal quantum efficiency is also predicted using PC1D to achieve more than 90% as shown in Fig.3.

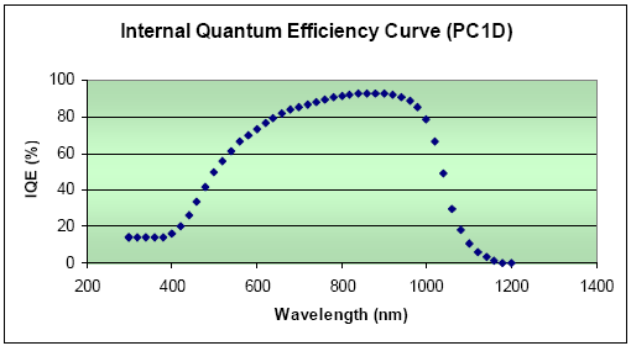

Fig.3 Internal Quantum Efficiency modelled by PC1D

III. CHARACTERISATION AND FABRICATION

Before the fabrication of the cells, characterization of material performance was conducted for minority carrier life time and emitter saturation current (Joe) at equivalent 1 sun intensity after each process step. Characterization process is shown in table 1.

Table 1 Sequence of Characterization Process

Step	Detail
Diffusion	Emitter formation
Oxidation	Grow thin passivation oxide
LPCVD	Deposit AR coating
Diffusion	n++ formation
Oxidation	To form diffusion barrier
Diffusion	p+ formation
FGA 1	Forming gas annealing to promote hydrogenation
FGA 2	Forming gas annealing to promote hydrogenation

Figures 4 illustrate that the adequate life time of around 560µs was maintained after all processes. From the graph it can be seen that life time has dropped sharply after heavy phosphorous diffusion and subsequent annealing is just enough to maintain the life time.

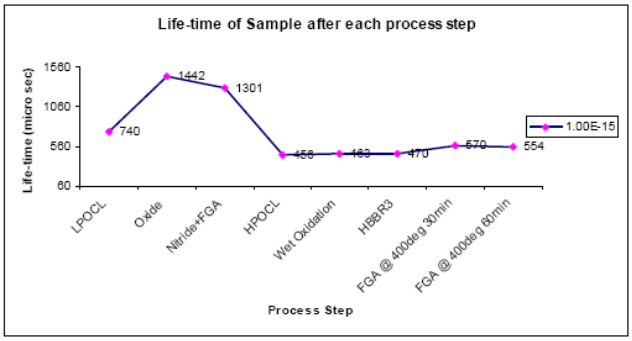

Fig.4 Characterization of Minority Carrier Life Time after each Process Step

Values of surface recombination were kept low throughout the process except after the heavy phosphorous diffusion. Value of emitter saturation current was maintained at around 25 fA/cm^2 after the last processing step. Figure 5 illustrates the characterization of Joe.

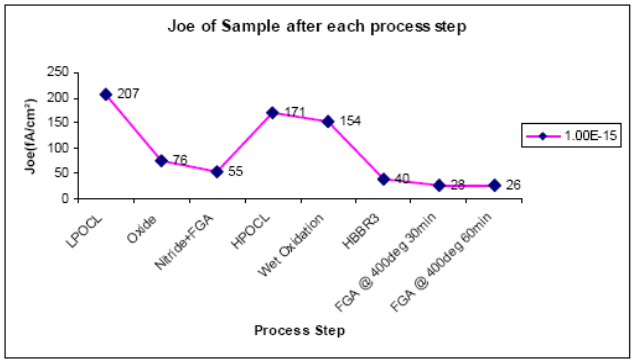

Fig. 5 Characterization of Emitter Saturation Current

Cells were fabricated using standard silicon process techniques, as shown in the table 2. Completed cells were diced out from wafer to form individual cell. Figure 6 shows the completed cell before dicing.

Table 2 Fabrication of silicon solar cells

Step	Detail
Si Etch	HF:HNO etch
RCA Clean	To clean organic/inorganic contaminant
Oxidation	Thick oxide for diffusion barrier
Photolithography	To make opening for diffusion
Laser Scribe	Create slots through the wafer
Diffusion	Emitter formation
Oxidation	Grow thin passivation oxide
LPCVD	Deposit AR coating
RIE	Make opening for n++ diffusion
Diffusion	n++ formation
RIE	To make opening for p+ diffusion
Diffusion	p+ formation
Metallization	Deposit metal Cr/Pd/Ag
Sintering	To form good ohmic contact
Dicing	To cut cells in individual
Testing	I-V testing

IV. TESTING

After dicing, individual cells were wired with electrodes on both sides of n and p regions. Cells were tested with current voltage flash tester under 1 sun illumination condition. Of many cells, the best performing cells are selected for further characterisation. Cells tested are observed to have high shunt resistance but significant series resistance, as shown in figure 7.

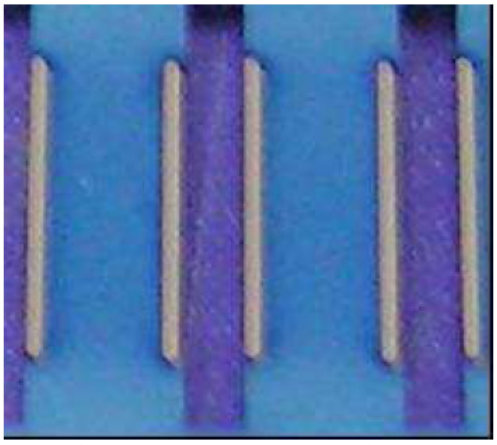

Fig. 6 Completed Si solar cells before dicing

Series resistance is caused by inadequate ohmic contact formed between the metal and diffusion. Table 3 illustrates the values of open circuit voltage, short circuit current and fill factor of the cells tested without having spectral filtering (eg using a GaAs cell).

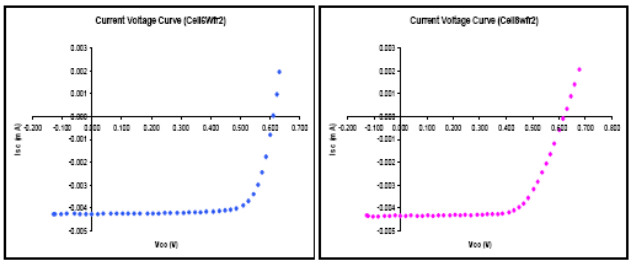

Fig. 7 Result of current-voltage for cells tested with I-V flash tester

Table 3 Voc, Isc and FF of Cells tested

	Voc (mV)	Isc (mA)	FF 9%)	Eff (%)
Cell6wfr2	612	4.25	75.9	16.5
Cell7wfr2	619	4.10	27.4	5.79
Cell8wfr2	619	4.34	66.2	14.8
Cell9wfr2	610	4.00	54.9	11.2

V. CONCLUSIONS

Cells have been completed that demonstrate the absence of shunts and a good fill factor. However, the open circuit voltage and current are low compared with the results expected from modeling. There were known problems with the processing which will be fixed in subsequent batches, which is likely to lead to sharply improved efficiency.

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