Solar Energy Materials and Solar Cells 172 (2017) 55–58

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Recombination-free reactive ion etch for high efficiency silicon solar cells

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ARTICLE INFO

Keywords:
Photoconductance decay (PCD)
Plasma radiation damage
High efficiency Interdigitated back contact (IBC) silicon solar cells
Recombination-free Reactive Ion Etch (RIE)
Lifetime degradation
Photoconductance decay PCD

ABSTRACT

Carrier lifetime degradation of reactive ion etch-processed silicon samples are investigated. Two types of carrier recombination: reversible and irreversible degradations induced by reactive ion etching (RIE) are identified. Irreversible carrier recombination is due to surface damage created by the RIE process that propagates a few microns deep into the silicon substrate. Reversible carrier recombination, on the other hand, is found to be caused by radiation damage when RIE etches only into the silicon oxide, and nitrogen annealing can restore the degraded carrier lifetime. A recombination-free RIE process is then developed in combination with a passivation stack consisting of silicon dioxide and silicon nitride layers. This improved RIE process is applied to the development of high efficiency silicon solar cells resulting in a conversion efficiency exceeding 24%.

1. Background

Reactive ion etch (RIE) is widely used in microfabrication and micromachining due to its highly directional etch capability, ability to transfer lithographically patterned complicated features to the underlying layers, lack of dangerous wet chemicals, cleanliness, and compatibility with vacuum-based fabrication processes. [1–3]. It has been extensively used in the fabrication of nanopores in silicon [4], memory devices [5], multilevel interconnect Si devices [6], photonic crystals [7,8], three-dimensional micro- and nanostructures [9] and microelectromechanical systems [10]. The benefits of RIE have been realized in the photovoltaic (PV) industry as well, particularly in the area of surface texturing to enhance light absorption and improve the solar cell performance. Traditionally, wet chemicals containing alkaline and acidic solutions are used to create pyramidal textured [11] and honeycomb shaped structures [12] to increase the light absorption. However, the large amount of silicon removed (~20 μm per side) during the texturing and surface damage etch by wet chemical processes poses a significant challenge when PV manufacturers move toward thin crystalline silicon solar cells. Compared to wet chemical process, RIE offers several advantageous: compatibility with thin crystalline silicon solar cells [13], independence of crystallographic orientation [14], and very low reflectivity on the textured surface [15]. Advances in RIE have been concentrated into the development of surface texture to further reduce the front surface reflectance. One of the significant attributes emerged from the RIE is the black silicon surface texture, which greatly modifies the silicon into needle-shaped surface structures resulting in very low reflectivity and high absorption of the light in the blue response region [16]. Black silicon structures have been applied in the development of high efficiency laboratory [17] and industrial silicon solar cells [14,15]. Despite those benefits, RIE generates defects near the surface of the semiconductor [18,19], consequently degrading the electrical performance of solar cells and other devices [20–25]. Defects and increased recombination induced by the RIE has limited the high efficiency potential of silicon solar cells, with only a handful groups demonstrated the incorporation of RIE into the development of silicon solar cells [25–29]. This contribution presents types of carrier lifetime degradation induced by RIE process and techniques to reverse the degradation. In addition, a novel technique was developed to circumvent the lifetime degradation induced by RIE in the process of etching the dielectric and passivation layers. Finally, this technique has been applied in a chain of high efficiency silicon solar cells developments achieving the conversion efficiency higher than 24%.

2. Experimental details

RIE was performed in an Oxford PlasmaLab80 system using CHF_3 plasma with the addition of O_2. The process pressure was 55 mTorr and the total gas flow rate was kept constant at 55 SCCM (cubic centimetre per minute at STP). Samples were placed on the water-cooled (25 °C) bottom electrode that was powered by a 13.56 MHz RF generator. The parallel upper and lower electrodes are 240 mm in diameter. The RF powers reported are forward powers, as the measured reflected power was insignificant. The RF power of 200 W and the dc bias of 450 V were used in this study. P-type float zone < 100 > 100 mm diameter low resistivity (1–5 Ωcm) silicon wafers were used in the experiments. Silicon dioxide (SiO_2) and silicon nitride (SiN_x) was grown in thermal oxidation and low pressure chemical vapor deposition (LPCVD)

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http://dx.doi.org/10.1016/j.solmat.2017.07.008
Received 31 March 2017; Received in revised form 7 July 2017; Accepted 10 July 2017

furnaces. Oxidation was done at 1000 °C for 30 min, followed by nitrogen anneal at the same temperature for 30 min. In the SiN_x deposition, the reactant gases – dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) were introduced into one end of a furnace tube, and pumped out from the other end. Deposition temperature and process pressure were maintained at 787 °C and 450 mTorr during the operation. Prior to the dielectric passivation of SiO_2 and SiO_2/SiN_x stack, samples were etch-polished, cleaved into quarter-piece samples and cleaned in RCA SC1 and SC2, followed by etching the samples in dilute HF (10%) to make the sample surface hydrophobic. The samples were then either thermally oxidised or grown in the LPCVD furnace, followed by forming gas annealing (FGA) in 10% hydrogen in nitrogen at 400 °C for 30 mins. Effective carrier lifetime was measured at an injection level of 10^{14}–10^{15} carriers per cm^3 using the quasi steady state photoconductance decay (QSSPCD) technique based on Kane and Swanson technique, assuming an intrinsic carrier concentration of $n_i = 8.95 \times 10^9\ cm^{-3}$ (at 297 K). Carrier lifetime represents bulk and surface recombination. Thickness of the SiO_2 and SiN_x films were measured by the filmetrics based on the spectral reflectance technique that analyses the reflected light perpendicular to the films. In the interests of experimental simplicity and clarity, no surface phosphorus diffusion (to suppress surface recombination) was used. Surface conditions of samples before and after RIE process were also measured and analysed by scanning electron microscopy (SEM). The RIE etch rate on Si (38 nm/min) was determined by first creating the mesas etch pattern, and then measuring the etch depth of mesas etch pattern by the alpha-step stylus profilometer; while that for SiO_2 (44 nm/min) and SiN_x (62 nm/min) was by the filmetrics before and after RIE.

3. Results and discussion

3.1. Reactive ion etching into silicon

RCA cleaned silicon samples were oxidised, annealed in FGA, and then etched by RIE at 200 W for 6 min. The RIE etch process time of 6 min was sufficient to remove all of the oxide and to etch a fraction of silicon. After etching into the silicon, all samples were again cleaned in RCA solutions and re-passivated by thermal oxidation. Effective carrier lifetime of samples was measured before and after RIE. Substantial lifetime degradation was observed for post-RIE etched samples and the degraded lifetime could not be recovered by subsequent FGAs (see Fig. 1). Fig. 2 further shows SEM pictures of samples before and after RIE process, and post-RIE samples were associated with significant

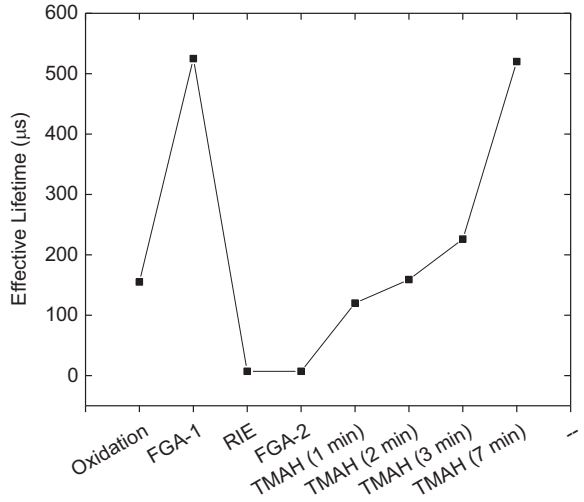

Fig. 1. Lifetime of samples after different process conditions. Carrier lifetime measurements were undertaken at the carrier injection of $1 \times 10^{15}\ cm^{-3}$, except for RIE and FGA-2 that were measured at $1 \times 10^{14}\ cm^{-3}$.

surface damages. These surface damages have been caused by the energetic ion bombardment during RIE process, consequently resulting in recombination-active defective surface. The passivation oxide of these RIE-processed sample was stripped in dilute HF, and then etched in TMAH (Tetramethylammonium hydroxide) at 90 °C for varying times. Approximately 0.3–0.4 µm of silicon per minute is removed in 10% TMAH at 90 °C. After etching in TMAH, the samples were cleaned in RCA solutions and re-passivated with SiO_2, followed by annealing in FGA. The aim of this work was to understand whether the RIE-induced damage is shallow or deep within the silicon. The fractional recovery of sample lifetime by etching in TMAH for 3 min is approximately 40%. A restoration of pre-RIE lifetime was achieved by increasing the TMAH etch time up to 7 min, which etched about 2–3 µm of silicon. The possible cause of RIE-induced damage propagating a few microns deep into the silicon substrate is explained by the cumulative lattice damage under the semiconductor surface caused by the continuous ion-bombardment during RIE [30,31]. Wet chemical etch could recover the degraded lifetime, however, it negates some benefits of RIE such as etch anisotropy and is undesirable if the solar cell fabrication is at the final stage.

3.2. Reactive ion etching into SiO_2

For the next set of RCA cleaned SiO_2 passivated samples the etch time of RIE was kept sufficiently short to etch only the SiO_2 layer, while avoiding to etch into the silicon. A wide variety of RF power (100 W and 200 W) and time (30 s and 60 s) were used for those samples. Lifetime degradation was still observed for all samples, although the degradation was considerably less than in the case where the RIE etch penetrates the oxide into the silicon. However, degraded lifetime of SiO_2 passivated samples where RIE enters the SiO_2 layer only was recovered to pre-RIE condition, following the FGA anneal (see Fig. 3). The similar recovery is observed by the nitrogen (N_2) annealing. The phenomenon of effective carrier lifetime recovery could be related to radiation damage. References have shown that radiation induced by plasmas generates trapping sites in oxide layers when exposed to RIE [32]. So long as the RIE etch does not penetrate into the silicon, the loss of the lifetime can be recovered by annealing in FGA or N_2. Rapid thermal anneal in N_2 ambient was also able to recover the degraded lifetime of SiO_2 passivated samples.

3.3. Reactive ion etching into SiN_x

SiN_x was further explored for RIE process. It was observed that when SiN_x was grown directly on the silicon the carrier lifetime was much lower than that grown with SiO_2. The cause of this has been due to the generation of defects in the silicon, induced by the mismatch in coefficients of thermal expansion between silicon and silicon nitride, together with its high extent of intrinsic stress, which may influence the carrier lifetime in the underlying silicon as well as the electron mobility [33]. Inserting a thin SiO_2 layer between SiN_x and the silicon provides a comparable or better passivation quality as SiO_2 grown sample [34]. Samples grown with a stack of SiO_2 (~20 nm) and SiN_x (~60 nm) were etched in RIE for 58 s. Note that ramp up and gas pressure stabilization steps during the RIE etch also remove a nanometer or two of SiN_x. The etch time was designed in a way to leave SiN_x with a thickness of 2 nm or less, without etching on a thin layer of SiO_2. In addition, a silicon shadow mask having a fractional exposure (i.e. 1%, 10% and 100%) was also used during the RIE process. The purpose of the shadow mask is to (1) identify if there is a varied degree of lifetime degradation exists with respect to the factional exposure, and (2) if limiting the RIE exposure to SiN_x would be necessary to mitigate the degradation. Fig. 4 shows the lifetime of SiN_x coated samples before and after RIE. As shown in the Fig. 4, pre- and post-RIE processed SiN_x coated samples were observed with negligible change in carrier lifetime for different degrees of fractional exposure. The reason for this could have been that

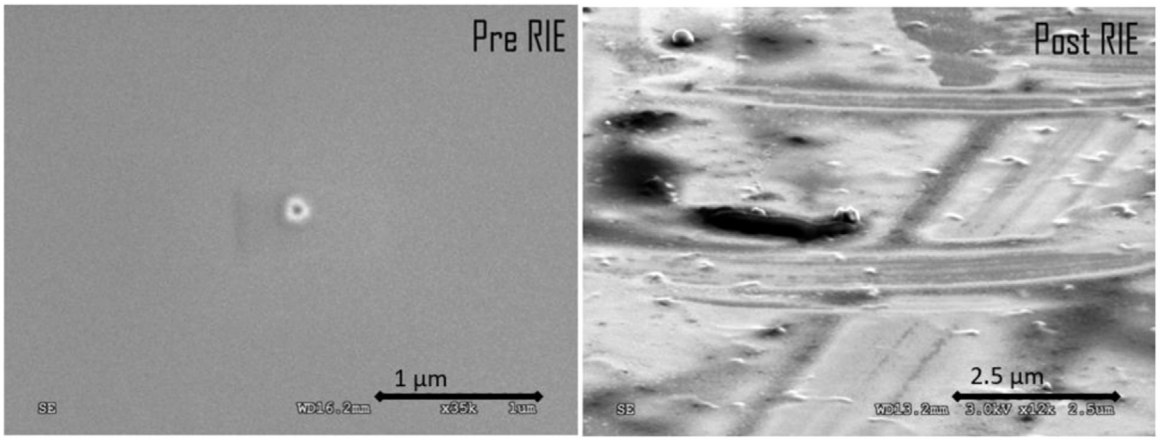

Fig. 2. SEM pictures of samples before and after processed by RIE. Pre-RIE SEM image was measured by almost 3 times higher magnification (i.e. x35k compared to x12k) than post-RIE SEM image. Even with the higher magnification, no surface defect or damage was observed on pre-RIE samples, but significant surface damages were observed on post-RIE samples, measured by the lower magnification.

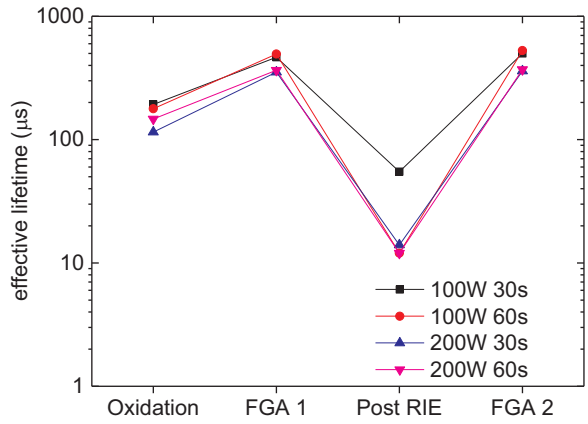

Fig. 3. RIE etching of SiO_2 only without penetrating into silicon. Lifetime was measured at the carrier injection of 1×10^{15} cm^{-3}.

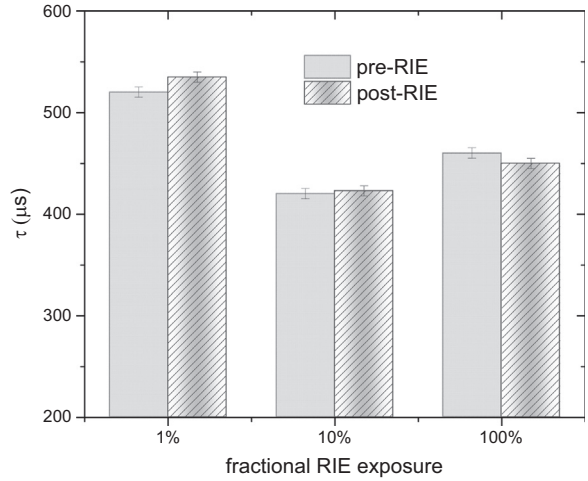

Fig. 4. Lifetime of SiN_x coated samples at the carrier injection of 1×10^{15} cm^{-3} before and after RIE, through the shadow masks with the fractional exposure of 1%, 10% and 100%. Lifetime measurements have the error percentage of ± 5%.

SiN_x layers are highly tolerant of plasma radiation, in contrast to SiO_2, and therefore neither nitrogen nor forming gas annealing was required subsequent to the RIE process to repair the radiation damage. The benefits of SiO_2/SiN_x stack—no carrier lifetime degradation during RIE, high tolerance to plasma radiation and higher etch selectivity compared to SiO_2 by RIE—in conjunction with well-controlled plasma etch offers the recombination-free RIE technique, which is well suited for the development of high efficiency silicon solar cells. Besides, requiring no annealing in N_2 or FGA on RIE-processed SiO_2/SiN_x stack shortens the fabrication process.

3.4. Integration of SiO_2/SiN_x passivation stacks in high efficiency silicon solar cells

The findings of irreversible carrier lifetime degradation of samples when RIE blasts through the silicon, radiation damage associated with SiO_2 grown samples when processed by RIE, high resilience of LPCVD SiN_x to plasma-induced radiation damage and good passivation provided by the SiO_2/SiN_x stack were taken advantage to successfully integrate RIE for the first time in a series of silicon solar cell developments—not just for the surface texture as other researches have been focusing on. Table 1 shows a list of high efficiency silicon solar cells developments incorporating the recombination-free RIE technique achieving conversion efficiencies up to 24.4%. RIE was employed repeatedly for a number of fabrication steps (i.e. contact opening, and selective removal of masks and diffusion barriers) in each cell development listed in Table 1. RIE-induced carrier lifetime degradation was effectively circumvented by employing a stack of SiO_2/SiN_x, assisted by the calibrated RIE etch to ensure that the plasma etch stops before SiO_2, but leaving a thin layer of SiN_x (~2 nm or less). The remaining layer of SiO_2 and SiN_x are comfortably etched off in wet chemicals (e.g. dilute hydrofluoric, *HF* acid) in a short amount of time. As in the publication, 19.2% efficient cell [35] incorporates heavy phosphorus diffusion (n^+ BSF) and boron emitter (p^+) at the rear, and a light phosphorus diffusion (FSF) at the illuminated front. The p^+ covers 75% of the rear surface, while the n^+ BSF covers 25% of the rear surface. No front surface texturing was employed in the 19.2% cell. A SiO_2/LPCVD SiN_x stack was used on both front and rear surfaces to provide dielectric passivation, anti-reflection (ARC) and insulation properties. Random

Table 1
High efficiency silicon solar cells developed by employing the technique of recombination-free RIE.

	Size (cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
Cell 1 [35]	16	682.0	35.00	80.5	19.20
Cell 2 [36,37]	13	680.0	40.30	80.1	22.10
Cell 3 [38]	13	681.0	40.80	80.7	22.45
Cell 4 [39]	4	702.5	41.95	82.7	24.37[a]
Cell 5 [40]	4	705.0	42.05	81.1	24.04
Cell 6 [40]	4	710.0	41.94	81.6	24.30

[a] Certified cell efficiency.

pyramidal textured front surface, doped and passivated with a light FSF and a SiO_2/PECVD SiN_x stack; was then incorporated in 22.1% and 22.45% [36–38] efficient cells, having the device pitch of 650 μm (i.e. n- to p-diffusion). The rest of the cells, with the conversion efficiency exceeding 24% [39,40], used the double layer anti-reflection (DLAR) coatings of PECVD SiN_x/PECVD SiO_x stack on the front and SiO_2/LPCVD SiN_x stack on the rear surface. The device pitch in these 24% efficient cells was further reduced to 500 μm.

4. Conclusion

Reversible and irreversible carrier lifetime degradation of silicon samples induced by RIE were presented. Irreversible carrier lifetime degradation of SiO_2 passivated silicon samples occurs when RIE etches through the silicon creating defects near the surface of the semiconductor, consequently degrading the electrical performance. Wet chemical etching can recover the damage induced by RIE etching into the silicon, but it negates some benefits of RIE such as etch anisotropy and is inconvenient in the cell development, especially in the final processing steps. Limiting the RIE etch within the SiO_2 layer instead of inflicting the etch into the silicon also causes the lifetime degradation, but this degradation is significantly reduced compared to etching into the silicon. This type of degradation is linked to the radiation damage, which is caused by the energetic ion bombardment during the RIE process. Radiation damage can be fully restored by annealing the degraded lifetime samples in FGA or N_2 environment. SiN_x coated silicon samples, on the other hand, show better resilience to the radiation damage than SiO_2 coated samples, with little or no lifetime degradation observed after RIE process. However, inserting a thin SiO_2 layer underneath the SiN_x is required to circumvent poor passivation quality induced by depositing SiN_x directly onto the silicon. Therefore, to maximize cell performance, a thin SiO_2 and SiN_x passivation stack is used in parallel with the calibrated RIE etch. This combination provides a recombination-free etch process that was successfully implemented in a range of silicon solar cell developments and resulted in a certified conversion efficiency exceeding 24%.

Acknowledgement

The author acknowledges the funding and support from the commonwealth government of Australia. Kris Davis for reviewing the manuscript.

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