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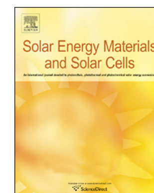

Simple and versatile UV-ozone oxide for silicon solar cell applications

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ABSTRACT

Semiconductor surface clean is sometimes perceived as costly but long recognized as pivotal in determining the final semiconductor device performance and yield. In this contribution, we investigated the effectiveness of crystalline silicon surface cleaning by a simple UV-ozone process in comparison to the industry standard RCA clean for silicon photovoltaic applications. We present a unique method of processing the silicon surface effectively by UV-ozone cleaning. Despite being simple, UV-ozone cleaning results in a superior surface passivation quality that is comparable to high-quality RCA clean. When used as a stack dielectric—UV-ozone oxide overlaid by aluminum oxide—the thickness of UV-ozone oxide plays an important role in determining the passivation quality. Of all treatment times, 15 min of UV-ozone treatment results in an outstanding passivation quality, achieving the effective carrier lifetime of 3 ms and saturation current density of 5 fA/cm^2. In addition, we present a simple and effective technique to extract values of electron/hole capture cross-section for the purpose of analyzing the interface passivation quality from already measured surface recombination parameters of saturation current density, interfacial trap density and total fixed charge, instead of measuring on the separately prepared metal-insulated-semiconductor (MIS) samples by the techniques: frequency-dependent parallel conductance or deep-level transient spectroscopy.

1. Background

Semiconductor surface cleaning is sometimes seen as a costly process as it consumes a significant amount of chemical resources and can require considerable waste disposal. However, it is accepted that an effective surface cleaning leads to improved device performance. Over the years, various types of crystalline silicon (c-Si) wafer cleaning sequences have been applied, based on the mixture of $NH_4OH + H_2O_2$, $HCl + H_2O_2$ and HF [1]; plasma etch [2], plasma treatment for small-geometry devices [3], chlorine cleaning [4] and hydrogen peroxide as an oxidant in the chlorine cleaning [5] to remove photoresist, contaminants, particles, organic/inorganic impurities and native oxide on the silicon wafer surface. Wafer cleaning chemistry, based on hot alkaline and acidic hydrogen peroxide solution—called RCA (Radio Corporation of America) standard clean—has been the primary method of cleaning in the microelectronic industry [6]. RCA standard clean includes the mixture of $NH_4OH/H_2O_2/H_2O$, referred as SC-1, and $HCl/H_2O_2/H_2O$, referred as SC-2. SC-1 removes the organic contaminants, while inorganic contaminants are removed by SC-2. Ultraclean deionized water is used for intermediate and final rinses after SC-1 and SC-2, respectively [1]. However, the SC-1 was found to cause the surface damage, due to micro-roughness formed by NH_4OH [7]. A new candidate, named "IMEC-Clean" to potentially replace the RCA clean was later introduced, enabling near-perfect removal of metallic particles [8]. The IMEC-Clean includes a mixture of H_2SO_4/H_2O_2, followed by a 1% diluted HF. The use of H_2SO_4/H_2O_2 mixture was also demonstrated in the development of Nanowire Solar Cells to increase the conversion efficiency [9]. Development of interdigitated back contact (IBC) silicon solar cells was also enabled by a cost-effective cleaning mixture of $H_2O/NH_3/H_2O_2$ with various chemical concentrations and different cleaning temperature. Recently, the application of ozone in wet and dry semiconductor surface cleaning processes has gained significant attention. Ozone has been extensively used in waste and swimming pool water treatment, water purification, medical sterilization, odor control and many other industries, due to its strong oxidizing ability. A reliable ozone generation based on the dielectric barrier discharge was first developed by Werner Siemens in 1857 [10–12]. Since then it has become the standard ozone generation technique in

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many industries including water treatment and semiconductor processing. Chen discussed benefits and applications of ozonated deionized water (DI-O_3) for wafer surface preparation in detail [13]. DI-O_3 research has already been reported by a number groups [14–16]. Bakhshi et al. also demonstrated the use of DI-O_3 in surface preparation prior to the application of single or stacked dielectric layers such as SiN_x, AlO_x, and AlO_x/SiN_x. This has resulted in the outstanding surface passivation achieving the saturation current density J_0 of 8 fA/cm^2 (per side) [17]. In addition to wet ozone cleaning, dry ozone cleaning based on the exposure of ultraviolet radiation is less complicated to operate and is effective in removing a wide variety of contaminants from surfaces. The ability of UV ozone in removing the organic layer such as photoresist polymer was reported as early as 1972 [18]. In 1974 Sowell et al. presented the UV cleaning of adsorbed hydrocarbons from glass and gold surfaces, in air and vacuum environment [19]. Also, in 1974 John Vig and his team also described through a series of experiments that UV-ozone cleaning is capable of producing clean surfaces in less than a minute [20]. Chemically cleaned silicon surfaces (such as after HF process) are at risk of particle contaminations and absorption of hydrocarbon from the ambient air, organic resists, etc.; therefore passivating c-Si surface with a protective coating such as UV-ozone oxide significantly reduces contaminations and hydrocarbon absorptions [21]. Studies have shown that UV-ozone oxide treatment leads to a significant reduction of carbon content in the subsequently grown dielectric films [22,23]. Moldovan et al. also presented the use of UV-ozone to remove fingerprints and glue on the c-Si wafer surface, and that conditioning 70 Ω/□ boron diffused layer with UV-ozone and passivating it with AlO_x/SiN_x stack achieved an emitter saturation current density of 49 fA/cm^2 [24]. The benefits of UV ozone have also been realized in organic photovoltaics. The use of UV-ozone to treat the ultrathin aluminum to form an alumina interlayer—between the active layer and indium tin oxide (ITO)—has been presented to improve electron extraction [25]. Treating the zinc oxide–poly vinyl pyrrolidone (ZnO-PVP) nanocomposite film used as an electron tunneling layer with UV ozone also improves the charge collections in dithienogermole–thienopyrrolodione-based polymer solar cells [26]. Besides the electron tunneling layers, treating the hole collection layer such as molybdenum trioxide (MoO_3) with UV ozone improves the surface morphology, transmittance and film quality [27]. Also, UV-ozone was demonstrated to change the highest occupied molecular orbital (HOMO) level of Phenyl-C61-butyric acid methyl ester ($PC_{61}BM$) [28]. In this paper, we present a novel method of cleaning the silicon surface by the UV-ozone technique in comparison to the industry standard RCA clean for application in silicon photovoltaics. We also employ a thin UV-ozone oxide (UV*o*) as an interface dielectric layer prior to the passivation of aluminum oxide (AlO_x) on c-Si samples. A deposition time of UV*o* interface dielectric was varied to optimize the passivation quality. We demonstrate that UV*o* technique is capable of providing both effective surface cleaning and outstanding passivation quality on c-Si silicon samples. In addition, we present a simple method to extract capture cross section values from already measured parameters of saturation current density J_0, interfacial trap density D_{it} and total fixed charge Q_{tot}.

2. Materials and methods

Planar 1–5 Ω cm n-type 250 µm Cz wafers were used in this contribution. Saw damage silicon etch was processed in Tetramethylammonium hydroxide (TMAH) at 90 °C, removing approximately 1 µm of silicon per minute. Effective carrier lifetime τ_{eff} and J_0 (per side) were measured using the transient photoconductance (PCD) decay technique at the excess carrier densities of 1×10^{15} and 5×10^{15} cm^{-3}, respectively. The measurement of J_0 undertaken at the carrier injection level higher than τ_{eff} is due to the fact that at regions, where the excess carrier densities are far greater than the substrate doping, maximizes the range of carrier lifetime's linear dependence on the carrier density, thereby distinguishing the surface from the bulk effects for the improved accuracy of J_0 analysis. J_0 is determined by the relation of $J_0 = \frac{qWn_i^2(\Delta n + N_d)}{2}(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}})$, where q is the electronic charge, W is the thickness of the silicon sample, n_i is the intrinsic carrier concentration, N_d is the bulk dopant concentration of the silicon sample, τ_{eff} is the effective minority carrier concentration and τ_{bulk} is the intrinsic bulk lifetime of crystalline silicon parameterized by Richter et al. [29]. Carrier lifetime represents bulk and surface recombination. Symmetrically passivated samples were used for measurement of τ_{eff} and J_0. RCA cleaning used a mixture of NH_3:H_2O_2:H_2O 1:1:5 and HCl:H_2O_2:H_2O 1:1:5 for the first and second cleaning step, respectively. UVo growth took place in Jelight 42 UV-ozone generator. In the ozone generator contaminant molecules and ozone absorb the short wavelength UV of 253.7 nm, and excite and simultaneously dissociate molecular oxygen at the wavelength of 189.9 nm. The photosensitized oxidation process happens when contaminant molecules react with atomic oxygen and so desorb from the surface. Recent technologies have made ozone cleaning process an extremely economical approach in both laboratories and industry. Using this technique, we have formed a thin layer of SiO_x on our samples. Dielectric layers (SiO_x, AlO_x, and RCA oxides) were removed in dilute (10%) HF prior to re-passivation. The thickness of UV*o* (or thin SiO_x) and AlO_x were measured by spectral ellipsometry (M-2000 J.A. Woollam) in a range of wavelength between 250 nm and 1200 nm. The measured signals are fitted using the Cauchy model. Based on the model, UV*o* oxides with the thickness of 1.5 nm, 1.7 nm, and 1.8 nm were achieved for 10 min, 15 min, and 20 min of process time, respectively. Deposition of AlO_x was by thermal atomic layer deposition (Cambridge NanoTech Savannah 100 ALD) with the deposition rate of 0.088 nm/Cycle at 200 °C. Annealing of UV*o*/AlO_x passivated samples was processed in the nitrogen ambient at 450 °C for 30 min. A contactless capacitance-voltage (C-V) measurement technique using PV2000 Semilab SDI instrument was used to characterize D_{it} and Q_{tot}. PV2000 tool dispenses charges on dielectric surface and measures surface voltage with vibrating Kelvin probe. Unless otherwise stated, D_{it} and capture cross section σ_n (or σ_p) reported in this contribution represent the values near the midgap. D_{it} and Q_{tot}—based on the contactless CV measurement—have the measurement uncertainty of 2% and 1%, respectively; while τ_{eff} and J_0 have the reported uncertainty of 3% [30,31]. Finally, nano-scale interface characterization was carried out with the help of transmission electron microscopy (TEM). For this purpose, cross-sectional TEM specimens were prepared by focused ion beam (FIB) milling technique using a FEI 200 TEM FIB. High-resolution TEM (HRTEM) images were obtained with the help of FEI Tecnai F30 TEM system at an operating voltage of 300 kV with a point-to-point resolution of 0.2 nm.

3. Results and discussions

First, n-type Cz < 100 > 1–5 Ω-cm samples were processed in TMAH to remove saw damage, followed by cleaning them in RCA solutions to make the surface hydrophobic. Post-TMAH processed samples have resulted with ~ 180 µm in thickness. Half of the samples were deposited with AlO_x having the thickness of 10–15 nm, while the rest were deposited with a very thin UV*o* (10 min of deposition) overlaid by the AlO_x of 10–15 nm. All samples were then annealed in N_2 ambient, followed by the PCD measurement. As shown in Fig. 1, the sample deposited by the UV*o*/AlO_x stack has notably improved τ_{eff} (i.e., 1554 µs compared to 1019 µs) and J_0 (7 fA/cm^2 compared to 11 fA/cm^2) than that by AlO_x alone. The passivation quality in terms of an effective surface recombination velocity, S_{eff} of the sample passivated by AlO_x only in this experiment is 8 cm/s, somewhat comparable the published result of 5 cm/s [32]. Here, S_{eff} is determined by the ratio of the wafer thickness to two times the τ_{eff}, assuming an infinite bulk lifetime time, as in published literature [32], and thus represents the upper limit. Typically, AlO_x effectively passivates the *c-Si* surface by the

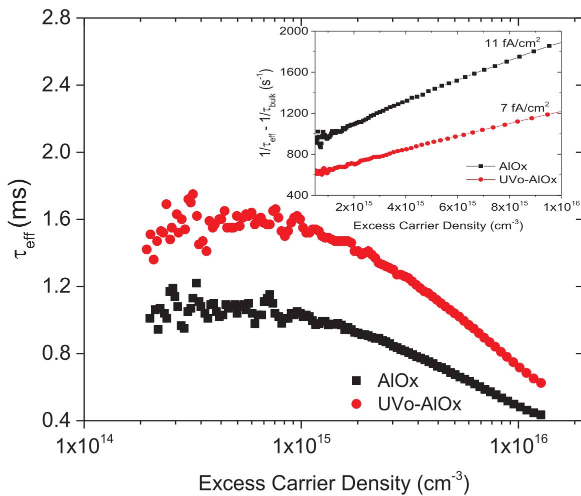

Fig. 1. Comparison of τ_{eff} and J_0 (inset figure) between samples passivated by AlO_x and UV*o*/AlO_x stack.

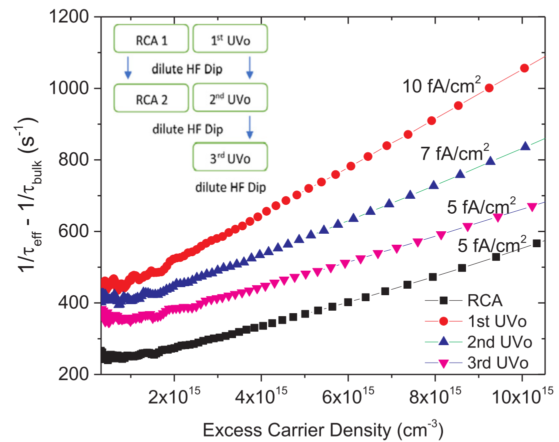

Fig. 3. Auger-corrected inverse τ_{eff} (Δn) of samples following RCA clean (1 & 2) and UV*o* clean (1st, 2nd, and 3rd). Inset indicates the cleaning sequence of samples that went through RCA and UV*o* clean.

combination of chemical passivation and field effect passivation, reducing the interface defect density and concentration of minority carriers near the surface, respectively [32]. While field effect passivation of AlO_x is driven by high negative built-in charge, the chemical passivation is owing to the interfacial SiO_x layer, grown intrinsically during the AlO_x deposition and annealing [33]. The results in Fig. 1 demonstrate that a high-quality interfacial layer formed using UV*o* provides superior passivation in comparison to the SiO_x grown intrinsically during the deposition and anneal of AlO_x.

Fig. 2 shows HRTEM images of samples deposited by AlO_x only and UV*o*/AlO_x stack. As in Fig. 2a, the SiO_x grown intrinsically during the AlO_x deposition has the thickness of 1–2 nm, which is in accordance with the published results [32,34]. However, SiO_x having a relatively higher thickness of ≈ 4 nm is observed in case of the sample subjected to UV*o* followed by deposition of AlO_x by ALD. (see Fig. 2b). This can be attributed to oxygen diffusion into Si during UV ozone treatment resulting in the formation of SiO_x interlayer, which further grows during the deposition of AlO_x by ALD. The relatively higher thickness of SiO_x in case of UV*o* deposited sample leads to improved surface passivation performance of the UV*o*/AlO_x stack, as compared to the AlO_x only. This statement is further supported by the discussion of capture cross section presented in the later part of this contribution.

To investigate whether UV*o* technique can be used as an effective surface cleaning technique, in comparison to the industry standard of RCA clean, an experiment was carried out by subjecting the saw-damage etched n-type low-resistivity sample to the 15 min of UV*o* growth on both sides of the sample. This sample was named as 1st UV*o* sample. Another saw-damage etched n-type sample was subjected to cleaning in RCA1 and RCA2 solutions, with dipping in dilute HF before and after RCA2, and then growing 15 min of UV*o* on both sides of the sample. To determine the effectiveness of surface cleaning, both RCA- and the 1st UVo-cleaned samples were then deposited with AlO_x (10–15 nm). Following the AlO_x deposition, samples were subjected to N_2 anneal and J_0 was extracted from the PCD measurement. J_0 of RCA cleaned sample was found to be lower than the first UV*o* sample (i.e., 5 fA/cm^2 versus 10 fA/cm^2 in the Fig. 3). Assuming the infinite bulk lifetime, RCA cleaned samples have achieved the S_{eff} of 3 cm/s—an equivalent to the published result [32]. The 1st UV*o* sample was then dipped in dilute HF to make the surface hydrophobic, followed with the process of growing and removing UV*o* (15 min) on the same sample and repeating these for another two times. These samples were named as 2nd UV*o* and 3rd UV*o* samples. Deposition of AlO_x and N_2 anneal was included after each UV*o* growth to assess the effectiveness of surface cleaning by the UV*o*. As shown in Fig. 3, subsequent deposition and removal of UV*o* have reduced J_0 further to 7 fA/cm^2 and 5 fA/cm^2, respectively, which have become comparable to that of the RCA cleaned sample. This improvement in J_0 is likely due to an effective oxidation of *c-Si* surface by the UV*o* technique and removal of UV*o* to make the *c-Si* surface free from contaminants. The purpose of AlO_x deposition and N_2 anneal included after each UV*o* clean was to assess the incremental improvement of post-UV*o* surface clean. A separate

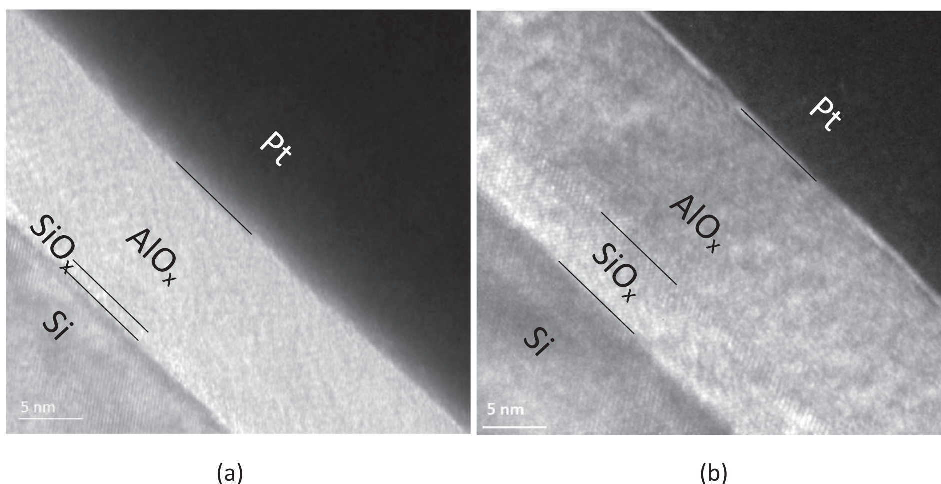

Fig. 2. HRTEM images of samples deposited with AlOx only (left figure) and with UV*o*/AlOx (right figure).

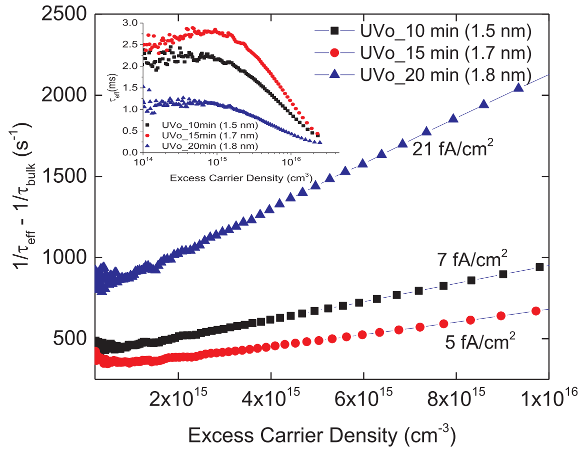

Fig. 4. Auger-corrected inverse τ_{eff} (Δn) and τ_{eff} (inset figure) of samples grown with 5, 10 and 15 min process time of UV*o*, resulting in thicknesses of in 1.5, 1.7 and 1.8 nm.

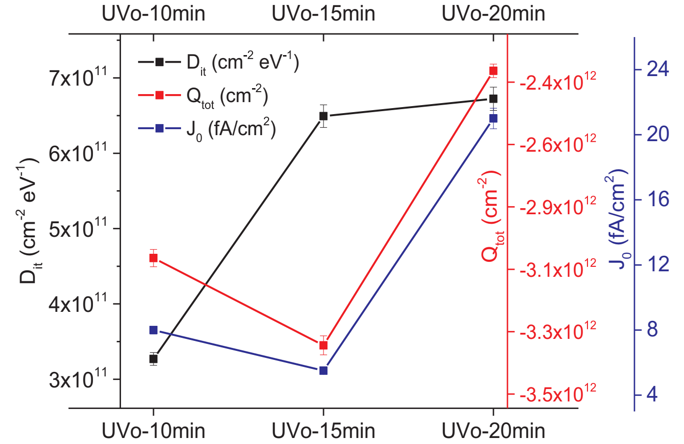

Fig. 5. Dependence of J_0, D_{it}, and Q_{tot} of samples grown with UVo of 1.5, 1.7 and 1.8 nm, respectively. D_{it} and Q_{tot} have the measurement uncertainty of 2% and 1%, respectively, based on non-contact CV measurement; while J_0 has the uncertainty of 3%.

experiment for the sample processed with just the UV*o* clean (i.e., deposit UV*o* and strip in HF) for three times—without AlO_x and N_2 anneal—showed the same reduction in J_0. This experiment demonstrates that a UV*o* clean aided by HF dip to remove contaminants in the grown UV*o* oxides can be used as an effective cleaning technique—an attractive alternative to the standard RCA cleaning, as it uses (1) less chemicals for the surface clean and also (2) alleviates the cross contamination of impurities—typically present in wet chemical processes—to the subsequently grown oxide, which in turn degrades the performance and yield of semiconductor devices [8,35–37].

Results in the aforementioned section demonstrate that in addition to providing the effective cleaning, UV*o* can be used in conjunction with passivation dielectric (e.g., AlO_x) to provide superior surface passivation. A further investigation was carried out when a thicker UV*o* was used. Saw damage etched n-type low-resistivity samples were grown with UV*o* for 10 min, 15 min, and 20 min, respectively; followed by deposition of 10–15 nm of AlO_x and N_2 annealing. The PCD measurement was undertaken to extract J_0 and τ_{eff}. As seen in Fig. 4, an increased thickness of UV*o* (i.e., from 10 min to 15 min) have reduced the J_0 from 7 fA/cm^2 to 5 fA/cm^2. However, an additional increase of UV*o* deposition time longer than 15 min has resulted in a significantly increased J_0 of 21 fA/cm^2. Possible reasons for this could have been due to (1) the increased thickness of UV*o* has diminished the field passivation effect of shielding the minority carriers from the interface between *c-Si* surface and UV*o*, and/or (2) degradation of film passivation quality owing to prolonged UV exposure. τ_{eff} of samples (see inset of Fig. 4) deposited with different UV*o* deposition times follow the same trend as the J_0.

A nondestructive corona/Kelvin probe measurement (contactless C-V) was then used to further characterize the interface passivation quality of the UV*o*/AlO_x stack [38,39]. The contactless *C-V* technique is used to determine interface defect density near midgap (D_{it}), which indicates how well the dangling bonds are passivated, and total fixed negative charge (Q_{tot}), which establishes the electric field that in turn minimizes the minority carrier concentration near the surface, thereby reducing the recombination [40]. Fig. 5 shows the dependence of J_0 on the interface parameters of D_{it} and Q_{tot} of samples grown with UV*o* of different thicknesses (1.5, 1.7 and 1.8 nm). As shown in Fig. 5, of all deposition times the sample with UV*o* of 1.5 nm have resulted in the lowest D_{it}. Increasing the thickness of UV*o* from 1.5 nm to 1.7 nm has sharply increased the D_{it} by about two-fold, but the D_{it} increase was saturated with further increasing the thickness of UV*o* to 1.8 nm. The increase of D_{it} as a result of increasing the deposition time of UV*o* (i.e., from 1.5 nm to 1.7 nm) is likely due to the degradation of the film quality at the expense of prolonged UV exposure. However, further investigations are required to determine why the D_{it} increase is saturated beyond 1.7 nm of UV*o* thickness. Q_{tot}, on the other hand, has barely changed (i.e., -3.0×10^{12} and -3.4×10^{12}) between the UVo thickness of 1.5–1.7 nm, but notably when the UV*o* thickness was increased beyond 1.7 nm. J_0 was also observed to notably follow the trend of Q_{tot} with respect to changes in the UVo thickness. C-V results in Fig. 5 indicate that Q_{tot}, rather than D_{it}, apparently determines the passivation quality of UVo/AlO_x stack. The following section further quantifies if the surface passivation of the n-type c-Si by the UV*o*/AlO_x is dominated by Q_{tot} or D_{it}.

An effective surface recombination can be determined by two parameters: effective surface recombination velocity S_{eff} and surface saturation current density J_0. A detailed discussion has been presented by McIntosh et al. [41] that J_0 is a superior metric, compared to S_{eff}, to quantify the surface passivation for undiffused silicon, since for the c-Si at 300 K in low-injection J_0 is independent of surface dopant concentration N_s when the surface charge $Q^{1.85}/N_s$ is greater than 1.5×10^6 cm for the inversion. This boundary condition is analogous to the experimental conditions in this contribution. The relationship of J_0 to the D_{it} and Q derived from [41] is given as:

$$J_0 = qS_{n0}2kT \in_{Si} n_{ie}^2/Q^2 \quad (1)$$

where q is the electron charge, T is the temperature at Kelvin, S_{n0} is the surface recombination parameter of electrons, n_{ie} is the effective intrinsic carrier concentration, ϵ_{Si} is the permittivity of silicon, and Q (q/cm^2) is the charge within the semiconductor that is invoked to balance the sum of the charge in the insulator and at the insulator–semiconductor interface. S_{n0} can be presented as:

$$S_{n0} = v_{th.n} D_{it} \sigma_n \quad (2)$$

where $v_{th.n}$ is the thermal velocity of electrons, σ_n is the capture cross section of electrons, and D_{it} is the defect density at midgap. σ_n and D_{it} in the equation are assumed as independent of energy. Parameterization of J_0 and S_{n0} can be found elsewhere [41]. Eqs. (1) and (2) can be used to determine the dependence of J_0 on S_{n0} and Q_{tot}, but σ_n is unknown and needs to be determined first. Generally, metal-insulator-semiconductor (MIS) structures can be measured either by the frequency-dependent parallel conductance [42] or time-domain capacitance transients using deep-level transient spectroscopy (DLTS) [43] to determine σ_n (or σ_p).

Preparation of MIS structures requires quite a number of process steps such as growing the insulation oxide (~ 10 nm of SiO_2 or thicker) on low resistivity (~ 1 Ω-cm or less) silicon substrate, single-sided removal of SiO_2, deposition of aluminum (~ 500 nm or thickness) on the

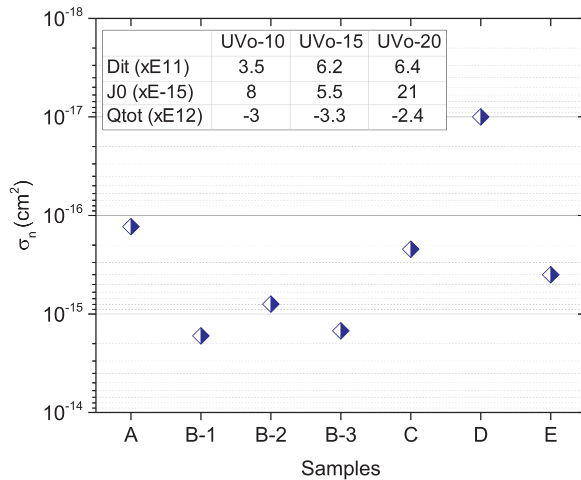

Fig. 6. Comparison of σ_n at midgap extracted by the Eq. (3) and reported in the literature. Inset table shows the parameters of J_0 (fA/cm^2), D_{it} (cm^{-2} eV^{-1}) and Q_{tot} (cm^{-2}) used for the extraction of σ_n (cm^2) at midgap for the samples grown with UV*o* of different deposition time: 10 s, 15 s and 20 s. The relationship of σ_n, J_0, D_{it} and Q_{tot} shown in the Eq. (3) is further derived from [41]. B-1, B-2, and B-3 samples represent UV*o*− 10, UV*o*− 15, and UV*o*− 20, respectively. A, C, D and E samples represent the published data.

SiO_2 and applying indium gallium (InGa) eutectic paste on the silicon to form contacts. Here, we present the alternate method of determining σ_n (or σ_p) values from already measured surface recombination parameters of J_0, D_{it}, and Q_{tot}, without the need to prepare MIS structures separately. Reorganizing the Eqs. (1) and (2), σ_n (or σ_p) can be written as:

$$\sigma_n = J_0 Q^2/2kTqv_{th.n}D_{it} \in_{Si} n_{ie}^2. \quad (3)$$

An analogous equation can be derived for σ_p. In Eq. (3) J_0, D_{it} and Q are values extracted from photoconductance and contactless C-V measurements, respectively, while the rest (k, T, q, $v_{th.n}$, ϵ_{Si} and n_{ie}) are known constant values; therefore σ_n can be determined. Fig. 6 shows the comparison between σ_n (see B-1, B-2 and B-3) extracted by the Eq. (3) and reported in the literature (A [44], C [45], D [46] and E [47]). As in Fig. 6, both σ_n extracted and reported in the literature are found to be comparable, only with some variations; which is not uncommon, based on the fact that measurement uncertainties (an order of magnitude [33,44]) exist with extracting σ_n (or σ_p) on typical MIS structures, and extracted σ_p (or σ_p) values depend on the normalized surface potential ν_s at which the measurement is made, thereby resulting in the significant error in σ_p (or σ_p) as a result of the error in determining ν_s [44]. By employing the extracted σ_p (or σ_p) in the Eqs. (1) and (2), the relationship of J_0 to D_{it} and Q_{tot} can be determined that Q_{tot} has a significant influence than D_{it} to J_0, due to its inverse of Q_{tot} square (1/Q_{tot}^2) relationship to J_0. Additionally, since measured D_{it} values are low or moderate, J_0 is strongly related to the concentration of charge Q_{tot} in the dielectric layer [48].

Using Eq. (3) along with the obtained D_{it} (7.5×10^{11} cm^{-2} eV^{-1}) and Q_{tot} (-4.8×10^{12} cm^{-2}) values from the contactless CV measurements and measured J_0 from Fig. 1; the σ_n of the sample deposited by AlO_x alone was further determined. The calculated values for σ_n of the UVo/AlO_x and AlO_x passivation stacks are 1.67×10^{-15} cm^2 and 2.7×10^{-15} cm^2, respectively, indicating that the UVo/AlO_x has an electron capture cross-section of 1.0×10^{-15} cm^2 lower in comparison to the AlO_x; further demonstrating its improved passivation quality of the thicker SiO_x formed by the UV*o*.

4. Conclusion

We presented a novel method of employing the UV*o* technique to effectively clean the c-Si surface. Not only is the UV*o* technique relatively simple and inexpensive, it provides an effective cleaning efficiency, comparable to the industry standard RCA clean technique, as it consumes less chemicals and minimizes the cross contamination of impurities from wet chemical processes. In addition to the effective surface cleaning, UV*o* provides the outstanding chemical passivation to reduce D_{it}. Passivation quality was found to vary with UV*o* thickness. When capped with AlO_x, 15 min of UV*o* processing time was found to be optimum, resulting in the τ_{eff} of 3 ms, J_0 of 5 fA/cm^2, D_{it} of 6.2×10^{11} eV^{-1} cm^{-2}, and Q_{tot} of 3.3×10^{12} cm^{-2}. We also identified that J_0 relates to Q_{tot} by the inverse of Q_{tot} square (1/Q_{tot}^2) while that to D_{it} by linear; as a result, the passivation quality of UVo/AlO_x stack on the c-Si is largely dependent upon Q_{tot} rather than D_{it}. In addition, the technique we presented to extract comparable σ_n (or σ_p) from already measured surface recombination parameters of J_0, D_{it} and Q_{tot} offers a simple and less-time consuming mean to the existing techniques of extracting σ_n (or σ_p) from the separately prepared MIS structures, for the purpose of analyzing the interface passivation quality. Implementation of unique surface clean techniques and passivation capabilities of UVo demonstrated in the contribution could lead to further improvement in surface cleaning and passivation quality, and they have emerged as potential low-cost alternatives to standard RCA clean in the photovoltaics industry.

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Competing financial interests

The authors declare no competing financial interests.

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