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Exceptional silicon surface passivation by an ONO dielectric stack

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ABSTRACT

Immeasurably low surface recombination of crystalline-silicon wafers is demonstrated with an oxide-nitride-oxide (ONO) corona charged dielectric stack. We detail experimental variations to each layer of the dielectric stack to establish a procedure which provides outstanding passivation properties on textured and planar silicon wafers. We demonstrate surface recombination velocities of < 1 cm/s and surface recombination prefactors of < 1 fA/cm^2, and we show that passivation remains stable over a 2-year period when stored in ambient conditions. The effective carrier lifetimes of n-type silicon are found to exceed the commonly accepted intrinsic lifetime limit, and in one case, a lifetime of 170 ms is attained. These high lifetimes indicate that ONO passivation is amongst the best dielectric passivation, and as such, might find applications in high-efficiency silicon solar cells.

1. Introduction

A number of silicon solar cell structures have surpassed 25% efficiency under one-sun illumination [1–3], with the current record being 26.6% [1]. One notable change that led to these very high efficiencies was improvement to surface passivation schemes, which involve either conventional dielectric films of aluminium oxide (Al_2O_3), silicon oxide (SiO_2) and silicon nitride (SiN_x) [2,4], heterojunction structures consisting of amorphous silicon (a-Si) or polysilicon (poly-Si) [1,2,5], or a combination of both [3]. These schemes involve chemically passivating the silicon surface, whereby the film adheres to silicon dangling bonds that would otherwise be electrically active. They also involve enhancing the surface passivation through the field-effect mechanism, whereby the films possess a large net charge ($> 10^{12}$ cm^{-2}) that repels either holes or electrons, thereby suppressing carriers from recombining at the surface. In this regard, excellent surface passivation is achieved through a combination of both chemical and field-effect passivation mechanisms.

Oxide-Nitride (ON) stacks have been extensively used in high efficiency solar cells as an anti-reflection coating (ARC) and passivation layer [4,6]. The silicon nitride when deposited atop thermal or native oxide, reduces the surface recombination significantly through hydrogenation and field effect passivation [7,8]. Corona charged ON passivation of undiffused silicon surfaces has been found to achieve a surface recombination prefactor J_{0s} as low as 0.36 fA/cm^2 on a 1 Ω.cm n-type silicon wafer [9,10]. ANU has demonstrated an interdigitated back contact (IBC) solar cell with the rear surface passivated using thermal oxide and low pressure chemical vapour deposition (LPCVD) of silicon nitride (Si_3N_4) to attain an efficiency of 24.4% [4].

Oxide-Nitride-Oxide (ONO) stacks have been widely used in the semiconductor industry for non-volatile computer memory to retain charge within the nitride layer [11]. Studies of plasma enhanced chemical vapour deposition (PECVD) ONO on solar cells have demonstrated thermally stable passivation and surface recombination velocity (S_{eff}) < 30 cm/s after a forming gas anneal [12]. Yet, to date, these film stacks have not been extensively explored for their surface passivation qualities and application to solar cells.

In this paper, we redefine ONO stacks with thermal silicon oxide, PECVD SiN_x followed by PECVD SiO_x. The thermal oxide provides the chemical passivation via a low interface-state density (D_{it}), the PECVD SiN_x carries positive charges and hydrogenates the Si-SiO_2 interface and bulk of the silicon wafer, and finally a PECVD SiO_x which retains corona

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charges and improves the overall optical properties of the stack in air. We will discuss the refinement of ONO films for the objective of surface passivation. We focus on passivation of n-type materials only, since this is now widely regarded as the material of choice for high-efficiency solar cells, owing chiefly to superior bulk lifetimes and thermal stability. Firstly, the thickness and post oxidation annealing (POA) of thermal oxide within the ONO film is investigated. The surface passivation on different deposition temperature of PECVD SiN_x are investigated on different crystal orientations and surface morphologies. We demonstrate the effects of positive corona charging on surface passivation and charge stability with further annealing to form an electret. Finally, we evaluate our refined ONO passivation electret on a range of n-type wafer resistivities and find that our ONO passivation scheme yields surface recombination prefactors $J_{0s} < 1$ fA/cm^2.

2. Experimental methods

We begin by detailing the baseline fabrication process sequences used for formation of ONO stacks: thermal oxidation, deposition of PECVD silicon nitride (SiN_x) and silicon oxide (SiO_x), annealing, and corona charging.

Prior to thermal oxidations and PECVD processes, {100} oriented n-type wafers were etched in tetramethylammonium hydroxide (TMAH) for 10 min at 85 °C to remove saw damage cleaned using the standard RCA process and subsequently dipped in a 1% hydrofluoric (HF) solution until the surfaces were hydrophobic. Thermal oxidations were conducted in a quartz tube furnace in oxygen ambient. The wafers were loaded at 700 °C and ramped up to 1000 °C at a rate of 15 °C/min. Upon reaching 1000 °C, wafers were annealed in nitrogen at the same temperature for 45 min followed by ramp down to 700 °C. The oxide thickness was measured to be 15 ± 1 nm using an ellipsometer (JA Woollam M2000D) [13].

Following thermal oxidation, amorphous SiN_x and SiO_x films were deposited by PECVD using an Oxford Instruments PlasmaLab 100 deposition tool. For SiN_x depositions, gas flowrates of 13 sccm of silane, 14 sccm of ammonia, and 980 sccm of nitrogen were used, with a deposition temperature of 400 °C, a chamber pressure of 650 mT and forward plasma power of 20 W, yielding an SiN_x thickness of 50 ± 3 nm and a real refractive index at 632 nm of ~1.93. PECVD SiO_x depositions were conducted at 250 °C with 9 sccm of silane, 710 sccm of nitrous oxide, and 161 sccm of nitrogen, producing films with a refractive index of 1.48 at 632 nm and a thickness of 90 ± 5 nm. We note, the thickness of SiN_x and SiO_x films were selected specifically for anti-reflection coating purposes based on simulation using OPAL2 [14]. Following the PECVD process, all wafers were subsequently forming-gas (FG) annealed at 400 °C in a quartz tube furnace for 30 min.

The ONO wafers were then positively corona charged in a conventional setup [15] without a mesh grid, using a steel needle with an applied voltage of 5 kV and an elevation of 8 cm above the samples. The deposition of surface charges was performed symmetrically on both surfaces and (except for the wafers of Section 2.4) the wafers were then subjected to an additional FG anneal at 400 °C for 30 min to embed the surface corona charges into the ONO dielectric stack [16–18]. The effective lifetime of the wafers was measured before positive corona charging and again after the anneal [17,18].

To ascertain the best ONO passivation procedure, each film underwent variations from this baseline to establish the best deposition conditions. Sections 2.1–2.3 details these variations and Fig. 1 illustrates the corresponding process flow.

2.1. Thermal oxidation thickness

We begin by investigating the impact of thermal oxide thickness. A 100 Ω.cm n-type FZ wafer with thickness of ~400 μm was cleaved into 4 quarters. The growth and depositions of ONO on all quarters were identical to baseline, except in this case the temperature of the oxidation was varied as stated in Fig. 1a. Each sample was loaded in oxygen at 700 °C and ramped up to different temperature set points. The samples oxide growth occurred during the ramp up to 850, 900, 950 and 1000 °C. Immediately after reaching the temperature set points, the gas flow was switched from oxygen to nitrogen and the wafers were subjected to further annealing at 1000 °C for 45 min.

2.2. Post oxidation annealing

To investigate the effects of post oxidation annealing in nitrogen, a 100 Ω.cm n-type FZ wafer with thickness of ~400 μm was split into 4 quarters. The growth and deposition of ONO on all quarters were identical to the baseline, except in this case the post oxidation annealing was varied as stated in Fig. 1b. The samples were loaded at 700 °C and ramped up to 1000 °C in oxygen. Upon reaching 1000 °C, the samples were annealed in nitrogen for 0, 15 and 30 min at 1000 °C and then cooled down in nitrogen. A control quarter without nitrogen annealing was loaded at 700 °C, ramped up to 1000 °C and ramped down to 700 °C in oxygen.

2.3. Deposition temperature of PECVD silicon nitride

To investigate the influence of SiN_x deposition temperature, several FZ and CZ n-type 100 Ω.cm silicon wafers featuring different surface conditions were used, these FZ being chemically polished {100} planar, FZ chemically textured using a TMAH-Isopropanol (IPA) mixture (rantex), and CZ mechanically polished {111} planar. Wafer thicknesses of {100} and {111} planar, and rantex surfaces were measured to be ~400 μm, ~420 μm and ~380 μm respectively. The growth and deposition of ONO on all wafers were identical to the baseline, except in this case the PECVD SiN_x deposition temperature was varied between 250 − 550 °C as stated in Fig. 1c. The deposition time was varied to keep the SiN_x thickness constant at different deposition temperatures. (As temperature increases, the deposition rate decreases and refractive index increases from 1.9 to 2.0 [19]). For antireflective purposes, we maintained an SiN_x and SiO_x thickness of 50 ± 3 nm and 90 ± 5 nm respectively, as outlined in the baseline procedure.

2.4. Corona charged ONO films

A 350 μm thick FZ n-type 100 Ω.cm silicon wafer was chemically textured using a TMAH and IPA solution mixture to form random pyramids [20]. The wafer followed the baseline ONO sequence, however in this case, the ONO stack was subject to sequences of corona charging for 10, 20, 60, 120 and 180 cumulative seconds. The lifetime of the corona charged wafer was measured by photoconductance decay after each successive charging period. During this experiment, unlike with the baseline process, the charges were not embedded in the ONO stack by a forming-gas anneal.

2.5. Measurement procedure

The effective carrier lifetime (τ_{eff}) was measured as a function of excess carrier densities Δn using a Sinton WCT-120 photoconductance instrument in transient mode. We report the effective lifetime ($\tau_{eff\_10^{15}}$) at $\underline{\Delta n} = 10^{15}$ cm^{-3} and maximum effective lifetime (τ_{eff_max}) within the Δn range of 10^{13}–10^{16} as an indication of the bulk lifetime. The surface recombination prefactor J_{0s} [21] was determined assuming the radiative recombination model of Nguyen [22] at 300 K, the Auger parameterisation of Richter et al. [23] (using equation 18 but omitting radiative recombination), and extracted using the method of Kane and Swanson [24,25]. The upper limit surface recombination (S_{eff_UL}) was calculated by assuming no recombination in bulk.

Capacitance-voltage (CV) measurements were undertaken to investigate the role of charge within the deposited films (before corona charging). The samples were 1 Ω.cm n-type polished silicon wafer of

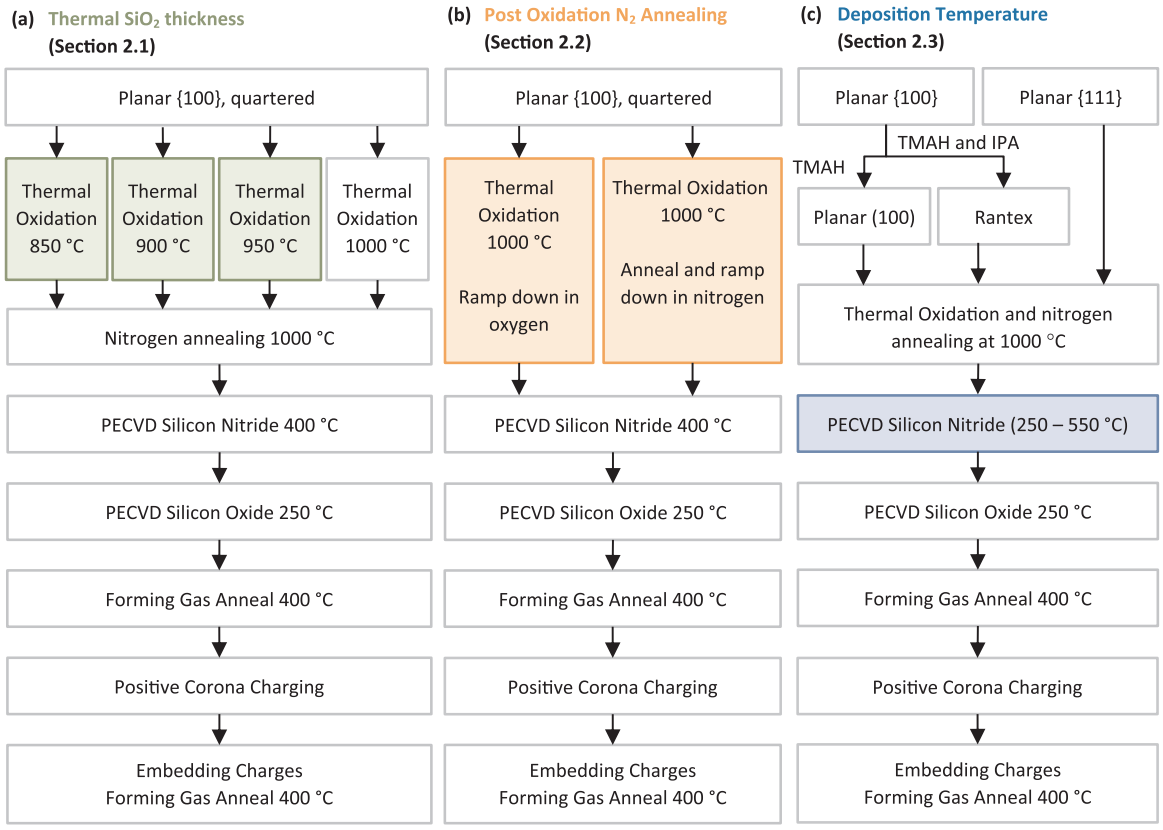

Fig. 1. Flow chart detailing the process variations to each layer (relative to baseline) in order to establish the best passivation conditions. (a) The baseline procedure is represented by the white boxes, while the variations to the oxidation temperature are highlighted in green. (b) The variations to the post oxidation anneal time and ambient are highlighted in orange. (c) The variations to the PECVD SiN_x deposition temperature is highlighted in blue.

{100} orientation passivated with ONO on the front, followed by the formation of MOS structures via thermal evaporation of aluminium dots on the front and full area aluminium evaporation on the rear. The effective charge (Q_{eff}) was then determined by high frequency CV measurements performed using HP 4284 A Precision LCR Meter sweeping voltages from –20V to 0V The area of the dot size was determined with a Nikon Eclipse LV150 Microscope. The flat-band voltage was determined from the flat-band capacitance [26] and converted into an effective charge density Q_{eff} by accounting for the work function difference between silicon (4.61 eV) and aluminium (4.2 eV) and by assuming that all charge is located at the Si–SiO_2 interface [27]. The possible contribution of capacitive and series resistance arising from rear contact were not accounted for during calculation of Q_{eff}. Thus, although the absolute value of the total charge is unknown, a relative comparison of Q_{eff} between samples is meaningful provided the location of charge (or more precisely, the charge centroid) within the ONO dielectric stack is the same for all measurements [28].

Kelvin probe (KP) measurements were undertaken using Single Point Kelvin Probe KP Technology. The wafers were 1 Ω.cm n-type polished silicon wafer of {100} orientation passivated with ONO on the front and full area thermal aluminium evaporation on the rear. The average of 100 consecutive measurements of the contact potential V_{KP} was taken at the middle of the wafer, and the voltage measured on a gold reference was used for calibration. The deposited charge density was then determined from V_{KP} by assuming all charge resided at the surface of the SiO_2. Calculation of charges were performed similarly in [18].

Fourier-transform infrared spectroscopy (FTIR) measurements were undertaken using Bruker VERTEX 80 v. Samples of 100 Ω.cm n-type polished {100} silicon wafers were dipped in hydrofluoric acid (HF) prior to the deposition of PECVD SiN_x. The FTIR instrument was calibrated and referenced with a similar bare polished silicon sample. All samples were scanned from 500 to 4000 cm^{-1}.

3. Results and discussion

3.1. The effect of varying thermal oxide thicknesses

The thermal oxide must be thick enough to assist surface passivation but not so thick that it significantly decreases optical transmission through the ONO [29,30]. Fig. 2 shows that a thermal oxide thickness of about 7 nm or greater (procedure outlined in Section 2.1) is sufficient to provide an exceptional level of surface passivation on undiffused 100 Ω n-type material. We do not discount the possibility that the variation in oxidation temperature affected the surface passivation, but we note a similar trend was observed by Kerr et al. [31] on thermal oxide and PECVD SiN_x (ON) structures in which they reported no correlation of passivation quality with thermal oxide thickness above 10 nm. Fertig et al. [32] observed similarly a decrease in emitter current recombination (J_{0e}) as thermal oxide thickness increases on light phosphorus diffused wafers passivated with thermal oxide and titanium dioxide stack.

3.2. The effects of post oxidation annealing

Post oxidation anneals (POA) are normally performed immediately after oxidation to reduce both the density of defect states [33–35] at the silicon/silicon oxide interface and charges within the oxide [36]. However, as shown in Fig. 3 for samples prepared according to the procedure outlined in Section 2.2, we do not observe any corresponding improvement in J_{0s} or τ_{eff} as the duration of the POA is increased. Instead, J_{0s} increases slightly from 0.2 to 0.5 fA/cm^2 and $\tau_{eff\_10^{15}}$ decreases slightly from 30 to 25 ms. We conclude that for these ONO samples, POA is not necessary and, if anything, increases

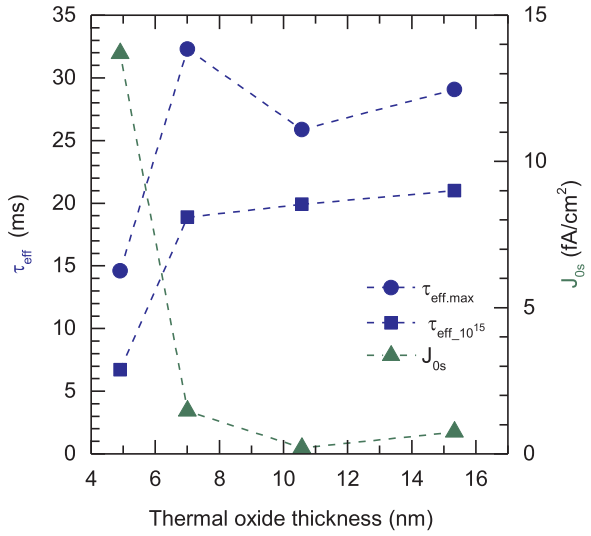

Fig. 2. Minority carrier lifetimes and surface recombination prefactors measured for ONO samples with different thermal oxide thicknesses, annealed at 1000 °C.

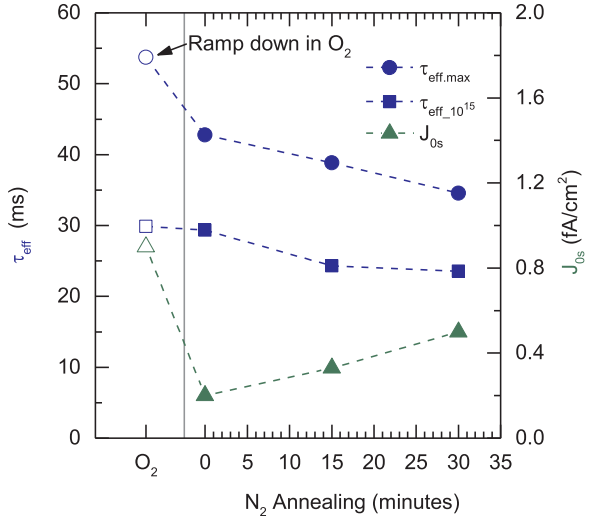

Fig. 3. Minority carrier lifetimes and surface recombination prefactors measured for ONO samples with different thermal oxide annealing times.

recombination.

The source of this reduction in lifetime and passivation quality might be considered to be caused by metal impurity contamination (e.g. Fe, Cr, Ni) during the nitrogen anneal [37]. Alternatively, the reduction in lifetime may be due to the re-introduction of vacancy-like defects back into the silicon bulk during the nitrogen anneal, as demonstrated by Abe [38].

Fig. 3 also shows that without any nitrogen annealing (i.e. when the ramp-down is performed in oxygen), the surface passivation is poorer (0.8 fA/cm^2 instead of 0.2 fA/cm^2), though still extremely good, while the maximum lifetime is even higher (55 ms instead of 43 ms). This observation reinforces the suggestion that the presence of a nitrogen-only ambient during anneal contributes to the formation of bulk defects.

These findings are consistent with the work of Grant *et al.* who demonstrated that vacancy related intrinsic defects (incorporated during FZ ingot growth) anneal out during a high temperature oxidation, thereby improving the bulk lifetime of FZ silicon [39,40]. Although an exact mechanism for bulk degradation resulting from the POA cannot be determined at this time, we have demonstrated that to

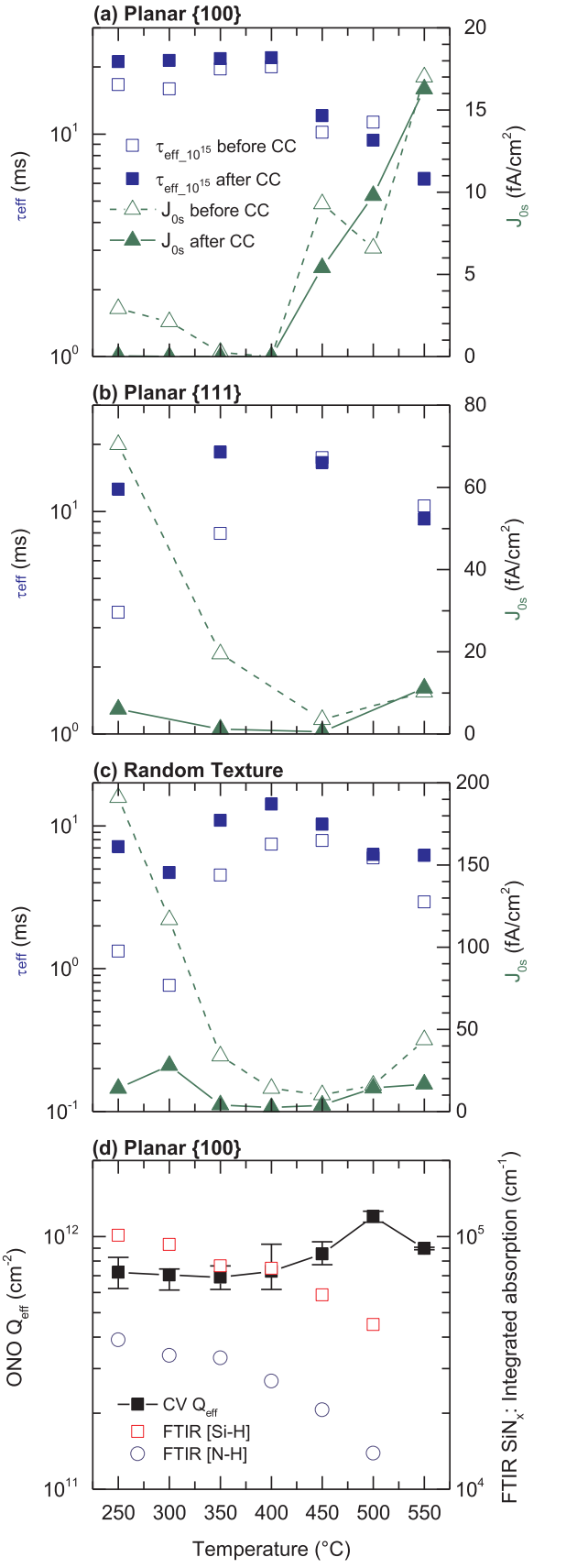

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Fig. 4. Effective lifetime $\tau_{eff\_10}{}^{15}$ and surface recombination prefactor J_{0s} ONO samples with different deposition temperatures of nitride on (a) {100}, (b) {111} and (c) rantex. $\tau_{eff\_10}{}^{15}$ measured at $\underline{\Delta n} = 10^{15}$ cm^{-3} before and after corona charging. Charge was measured using CV measurement on a 1 Ω.cm n-type {100} wafer as outlined in Section 2.5. Absorption for [Si-H] and [N-H] on silicon nitride were measured by FTIR.

achieve the highest lifetimes POA in nitrogen can be avoided.

3.3. Influence of PECVD silicon nitride deposition temperature

The important parameters during the deposition of PECVD SiN_x are radio frequency (RF) incident power, gas flow ratio, chamber pressure and temperature. The deposition temperature of PECVD SiN_x affects both the optical properties and deposition rate, similarly to gas ratio and chamber pressure [19,31,41]. In our investigation, we varied only the PECVD deposition temperature while keeping the gas ratio or the chamber pressure constant. The RF power was set to adequately ignite the plasma while reducing the possibility of plasma damage and ion bombardment [19]. Fig. 4a–c plot $\tau_{eff\_10}{}^{15}$ and J_{0s} as a function of deposition temperature from 250 °C to 550 °C, for samples passivated by ONO and for the various wafer crystallographic orientation and surface morphologies, as described in Section 2.3. The samples were subsequently subjected to positive corona charging prior to final anneal, in order to obtain the highest achievable lifetimes.

For the deposition temperature range in Fig. 4a–c, we were able to observe two different trends. Firstly, surface recombination decreases with increasing temperature over the range 250–400 °C. Secondly, surface recombination increases as the deposition temperature exceeds 450 °C. The decrease and increase of surface recombination with temperatures is similarly observed for a single layer nitride film on silicon [41,42], suggesting that deposition temperature of silicon nitride strongly influence surface recombination either as a stack atop of thermal silicon oxide or as a single passivation layer. The lowest J_{0s} (highest lifetimes) are achieved when the deposition temperature is within the range of 350–450 °C.

The decrease in J_{0s} with increasing deposition temperatures up to 400 °C suggests that either the density of electric charge in the films increases or that interface defect concentration decreases with temperature. The trend is particularly noticeable for {111} and rantex wafers, which have previously been found to exhibit higher interface states densities (D_{it}) than {100} surfaces [43–45], even after a forming gas anneal [45].

In order to determine the electrical properties of the ONO dielectric before corona charging, capacitance-voltage measurements were performed on {100} samples, as shown in Fig. 4d. Although thermal oxide grown on {100} orientated wafer has been reported to have lower charge than {111} [36,46], we assume the measured Q_{eff} trend for orientation {100} and {111} to be similar. The Fig. 4d indicates that Q_{eff} is relatively constant below a deposition temperature of 400 °C, despite the decrease in J_{0s} with temperatures up to ~450 °C. Assuming that the same trend occurs for all of the photoconductance samples of Fig. 4a–c, this indicates that the decrease in J_{0s} with deposition temperatures up to 450 °C arises due to a decrease in the interface defect density, rather than an increase in the charge density within the ONO stack. Although the mechanism in which SiN_x improves surface passivation isn't unequivocal, it has been reported that surface passivation from SiO_2 improves after capping it with SiN_x due to hydrogenation and positive charge [7,8,10]. Another possibility is that hydrogen molecules and radicals generated during deposition [47,48] passivate dangling bonds at the silicon/silicon oxide interface [7,49–52], causing a reduction in J_{0s}. The literature indicates that the common optimum temperature for hydrogenation by means of hydrogen plasma is 400 °C [51,52], which is in agreement with our observations. One other source of hydrogenation could be due to the deposition of SiN_x followed by subsequent annealing, which may release hydrogen into the bulk or interface of Si-SiO_2 [53–56].

In order to quantify the amount of hydrogen within the PECVD SiN_x film, FTIR measurements were performed on PECVD SiN_x samples to examine the concentration of Si-H and N-H bonds at 2150 and 3350 cm^{-1}. Fig. 4d plots the absorption over PECVD SiN_x thickness [57] of different deposition temperatures rather than absolute bond concentration values [58]. We find no clear dependence of J_{0s} on [Si-H], similar to Wan et al. for PECVD SiN_x [41]. In this regard, we postulate that as the bond density of Si-H and N-H reduces with deposition temperature, the released hydrogen could passivate the silicon surface resulting in a lower interface defect density at 400–450 °C. (The interface defect density could not be determined from low- and high-frequency CV measurements due to large measurement uncertainty in the low frequency measurement.)

After corona charging, J_{0s} decreases below 20 fA/cm^2 for almost all deposition temperatures and wafer types. In fact, for planar {100} samples, J_{0s} decreased to practically 0 fA/cm^2 for low-temperature depositions. The J_{0s} decreases most upon corona charging for deposition temperatures below 400 °C and little or not at all for deposition temperatures 450 °C and above. The cause of increasing J_{0s} above deposition temperatures beyond 450 °C remains uncertain as dehydrogenation [59] or fast diffusing contamination [37] could have occurred.

Surface passivation depends on crystal orientation and surface morphology, and furthermore, that the dependence is different for each dielectric film [45,60,61]. To investigate the surface recombination ratio between planar {111} to {100}, we define the ratio between the two as f_O (where subscript O stands for orientation). For example, Baker-Finch et al. [60] found that for $S_{eff.UL}$ at $\underline{\Delta n} = 10^{15}$ cm^{-3} on thermal SiO_2 planar {111} to be higher than planar {100}, with the ratio of f_O ~4, whereas Wan et al. [61] found surface orientation to be less influential for PECVD SiN_x with f_O ranging from 0.8 to 1.7 at $\underline{\Delta n} = 10^{15}$ cm^{-3}. The surface recombination at a rantex surface (which has {111} oriented facets) is normally higher than at a {111} planar surface due to its higher surface area ($\sqrt{3}$ times larger) and to possible stress-induced defects at concave and convex features [60,62]. The comparison of surface recombination ratio between surface area corrected rantex to planar {111} is denoted as f_V (where subscript V stands for vertices). Accounting for the differences in surface area, Wan et al. found that for SiN_x passivation (n = 1.93) has a higher $S_{eff.UL}$ of rantex over planar {111}, with f_V ~2 [61]. By contrast, for amorphous silicon f_V ~0.9 [61,63].

In this work, we compared f_O and f_V using S_{eff_UL} at $\underline{\Delta n} = 10^{15}$ cm^{-3} instead of J_{0s}. We found that f_O to gradually decreases with increasing SiN_x deposition temperature up to 350 °C. Before corona charging, the ONO with deposited SiN_x at 350 °C has f_O of ~2.6. After corona charging, the f_O reduces to ~1.2, making it more alike SiN_x than SiO_2. Thus, whether the crystal orientation is {100} or {111}, the influence of surface defects on ONO passivation is comparable, similar to PECVD SiN_x [61,63].

Similarly, we have found charged ONO f_V to gradually decrease with increasing SiN_x deposition temperature up to 350 °C. Comparing area corrected f_V before corona charging, the ONO with deposited SiN_x at 350 °C has f_V ~0.9. After corona charging, f_V remains at ~0.9. This is near enough to unity to indicate that the reason ONO passivation is poorer on the rantex samples compared to the {111} is due to their higher surface area, with minimal impact from the convex and concave aspects of the morphology.

3.4. Impact of corona charge

Corona charging of dielectric coated silicon provides a field-effect passivation that can be used to improve surface passivation by either accumulating or inverting the concentration of free carriers at the surface [17,18,64–66]. During the charge deposition, it is believed that

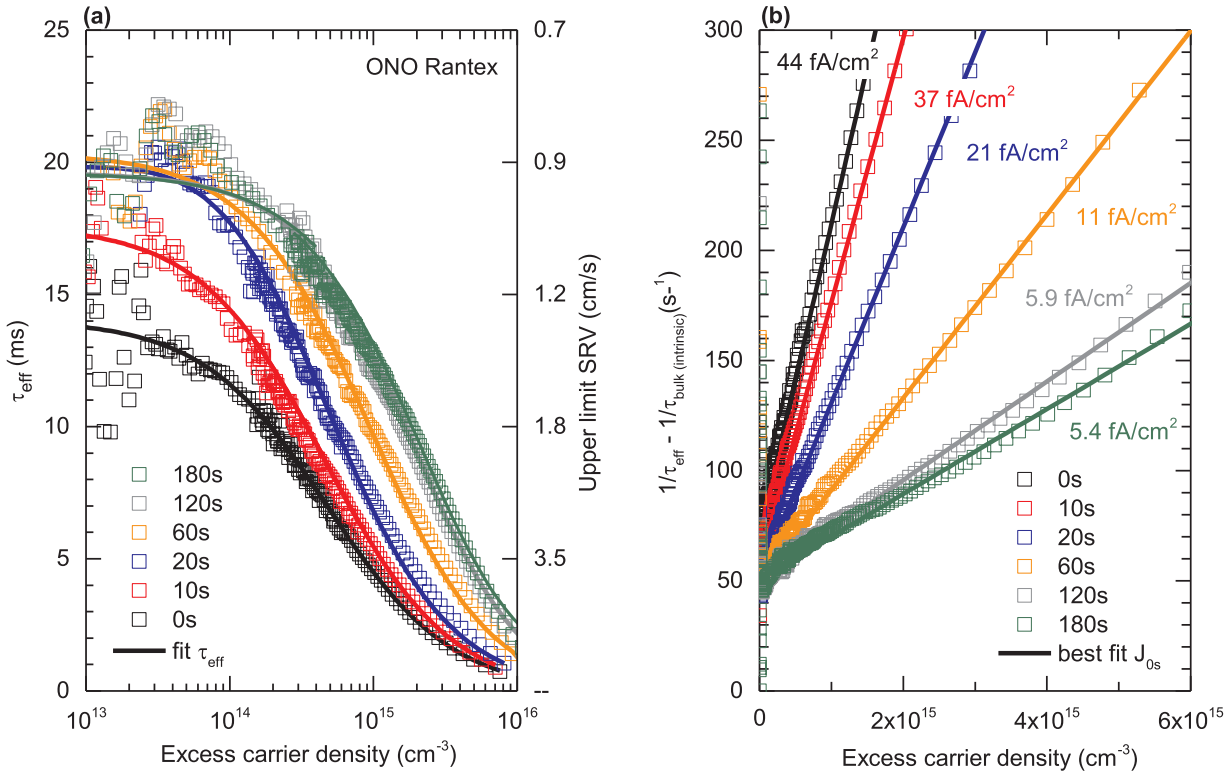

Fig. 5. (a) ONO on 100 Ω.cm n-type textured sample corona charged for an increasing cumulative period at 5 kV. Calculated upper limit SRV on secondary y-axis scale is not to scale. (b) Line plots showing the best-fit of J_{0s} for various levels of charging. Lifetime curves were modelled using SRH equation [69] and Auger parameterization [23].

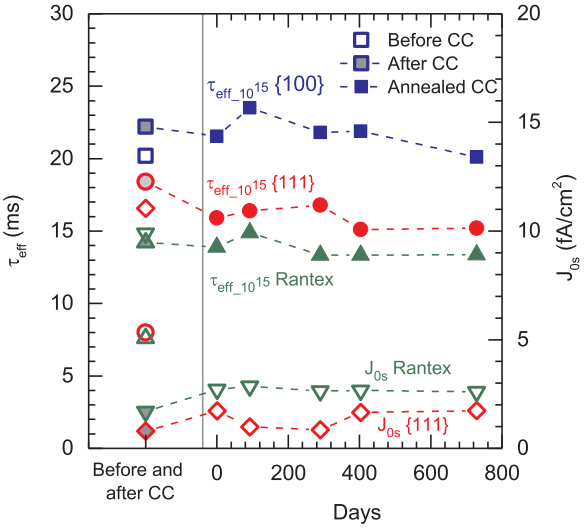

Fig. 6. Effective lifetime measured at $\Delta n = 10^{15}$ cm^{-3} and J_{0s} of corona charged samples plotted after FGA annealing and stored in ambient conditions up to 2 years. No data plots for J_{0s} of {100} sample as extracted values were lower than 0 fA/cm^2. The wafer thickness of {100} planar, {111} planar and rantex surfaces were measured to be ~400 μm, ~420 μm and ~380 μm respectively.

anion species of hydrogen, nitric oxide and nitrogen dioxide are generated whilst applying a large voltage across the needle [67,68]. Fig. 5a shows a family of lifetime curves for ONO samples subjected to different positive charge durations (as outlined in Section 2.4). Each successive corona charge led to a significant improvement in the effective lifetime at all excess carrier densities Δn. The lifetime saturates after corona charging for around 120–180 s as demonstrated by the lifetime measurement.

For comparison, Fig. 5a shows the conversion from effective lifetime to an upper limit surface recombination velocity ($S_{eff.UL}$) assuming an infinite bulk lifetime. Extremely low $S_{eff.UL}$ of < 1 cm/s are attained on randomly textured silicon surface after corona charging ONO for just 120 s.

Rather than τ_{eff} and $S_{eff.UL}$, it is preferable to quantify surface recombination with J_{0s} due to J_{0s} being independent of injection level when the surface is under accumulation [21]. Fig. 5b plots the measured J_{0s} (between 10^{14} and 10^{16} cm^{-3}) after successive corona charging up to 180 s, where no further improvements in τ_{eff} were observed. From Fig. 5b, there are two notable outcomes, the first relates to the 'linear' fit of each measurement, thereby indicating the surfaces are in accumulation, as expected from a positively charged dielectric on n-type silicon, and secondly, the results clearly show a substantial reduction in J_{0s} from 44 to ~5 fA/cm^2 after successive corona charging up to 180 s.

While the passivation is outstanding after corona charging, it is well known that this treatment is not stable, and the deposited charge can be removed by rinsing the samples in isopropanol (IPA) [17,18,70]. The benefit of a simple corona charge is therefore only temporary, and would not provide a long-term efficiency gain in finished devices. However, annealing corona charged samples have been found to embed surface charges into the dielectric [16–18]. To demonstrate the benefits of embedding corona charges into ONO, we have performed this treatment (samples from Experimental method 2.3) on {100}, {111} and rantex surfaces and monitored the stability for over a 2-year period in ambient conditions. Fig. 6 plots the results of wafers before and after corona charging and monitors annealed corona charged wafers after 400 °C in FGA. From the measured values for $\tau_{eff\_10}{}^{15}$ and J_{0s} shown in Fig. 6, we find corona charged samples had a slight increase in surface recombination after annealing due to the reduce overall charges [17,18]. It is evident that the passivation scheme is stable over a 2-year

Table 1
Measured lifetime parameters for a variety of n-type wafers with ONO, NO and SiN_x passivation. J_{0s} is extracted by fitting injection levels from 1 to 5 × 10^{15}. Values are reported at 300 K, where n_i is 9.7 × 10^9 cm^{-3}, $\tau_{eff\_10}{}^{15}$ at Δn = 10^{15} cm^{-3} and τ_{eff_max} at Δn from 10^{13} to 10^{16} cm^{-3}.

ρ_{bulk} (Ω.cm)	Type	Crystal Lattice	W (μm)	Surface	Passivation Layer	$\tau_{eff\_10}{}^{15}$ (ms)	τ_{eff_max} (ms)	J_{0s} (fA/cm^2)
0.50	CZ	100	155	Chem. P	ONO	3.2	3.7	–
1.07	CZ	100	272	Chem. P	ONO	12.4	15.1	–
1.77*	FZ	100	398	Chem. P	ONO	19.3	25.5	–
2.71	FZ	100	228	Chem. P	ONO	18.6	20.6	–
4.97*	FZ	100	388	Chem. P	ONO	34.9	43.7	0.2
8.93*	FZ	100	181	Chem. P	ONO	28.0	38.5	0.8
86.7*	FZ	100	291	Chem. P	ONO	72.5	170	0.3
142	FZ	100	382	Chem. P	ONO	44.9	84.6	–
115	FZ	–	350	Rantex	ONO	18.0	42.6	4.3
105	FZ	–	351	Rantex	[a] SiN_x	10.1	12.9	9.8
2.96	FZ	–	250	Rantex	[b] NO	4.3	4.5	4.7

Chem. P: Chemical Polish.
Rantex: Random texture.
[a,b] SiN_x Deposition technique: PECVD (Roth & Rau AG, system AK400).
[b] SiN_x deposited onto silicon wafer followed by PECVD SiO_x [4].
*Wafer resistivity measured at University of Oxford using Hall Coefficient measurement after thermal processing [71].
*Wafer was not subjected to step (iv) in Section 3.5.
All other wafer resistivities reported were based on dark conductance measurement using QSSPC before any thermal processing.

period, with no dependence on surface condition on each of the sample.

Kelvin probe measurements performed after corona charging shows positive surface charges of ~4.3 × 10^{12} cm^{-2} on an n-type planar 1 Ω.cm wafer. CV measurements performed before and after corona charging (with annealing to embed the charges), showed an increase in effective charge of Q_{eff} ~7 ± 2 × 10^{11} cm^{-2} to 2.4 ± 0.3 × 10^{12} cm^{-2} respectively. This increase in effective charge indicates that the deposited surface corona charges is driven deeper into the ONO dielectric stack after further annealing [28].

3.5. ONO passivation on different undiffused n-type dopant concentration samples

A summary of the foremost results obtained in this study using our advanced ONO passivation scheme as obtained on various wafer types, thickness and surface morphologies are compiled in Table 1. Taking the best conditions in each of the variations described above, the wafers featuring advanced ONO passivation were processed as follows;

(i) Ramp up from 700 °C to 1000 °C in oxygen and then ramp down to 700 °C in oxygen with no subsequent POA in nitrogen (12 ± 2 nm).
(ii) 400 °C PECVD SiN_x (50 ± 3 nm).
(iii) 250 °C PECVD SiO_x (90 ± 5 nm).
(iv) Anneal ONO in FG at 400 °C for 30 min
(v) Deposit positive corona charge at 5 kV on ONO passivated wafers for 120 s
(vi) Anneal charged ONO wafers in FG at 400 °C for 30 min to embed and stabilise the corona charges.

For reference purposes we included the recent best passivation results achieved using PECVD SiN_x and PECVD SiN_x and SiO_x films in our laboratory.

Fig. 7a plots the maximum effective lifetime measurements published in the literature on n-type samples. We find ONO passivation exceeds the lifetimes of various passivation schemes and achieves a record lifetime of 170 ms on a 100 Ω.cm n-type sample. Fig. 7b shows effective lifetime measurements of three different n-type resistivity

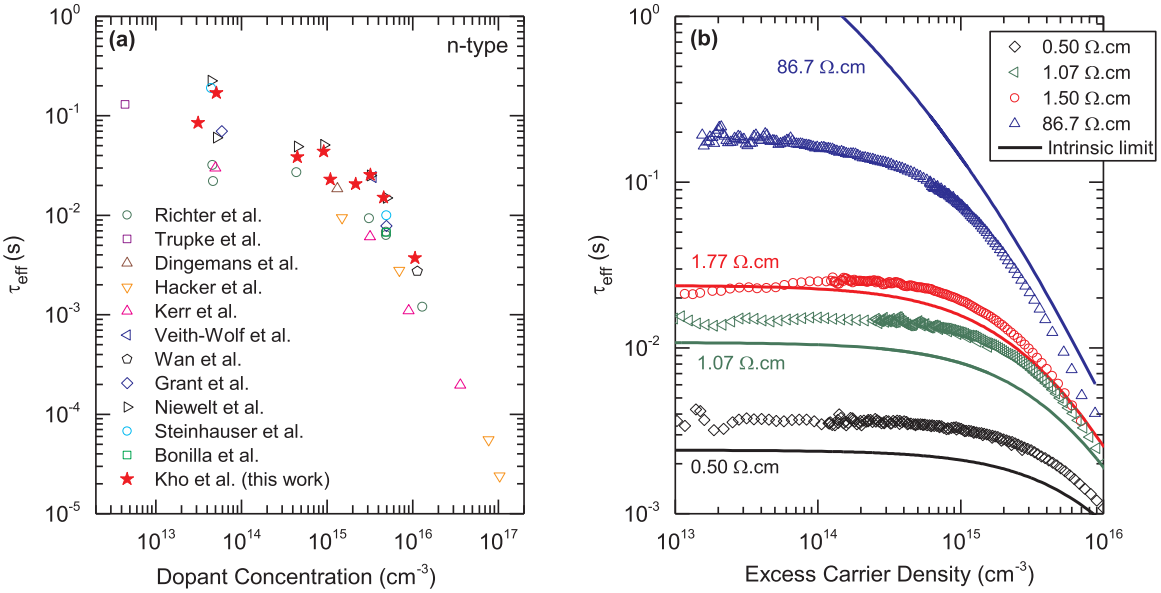

Fig. 7. (a) Maximum lifetime as a function of dopant concentration measured at 300 K on n-type silicon together with literature data (Refs [23,72–80].). (b) ONO passivation with a range of n-type silicon resistivity in comparison to intrinsic limit with parameterized Auger [23] including radiative recombination [22] (lines).

samples which exceed the commonly accepted intrinsic limits. This not only demonstrates the outstanding passivation quality of ONO, but it also highlights the necessity to revise the parameterised intrinsic limit for silicon

4. Conclusion

We presented a study into the surface passivation provided by ONO on different surface morphologies and crystal orientations. We have examined ONO electret passivation by investigating different oxide thicknesses by various oxide growth temperature, POA with nitrogen, PECVD SiN_x deposition temperature, corona charging and on a range of undiffused n-type dopant densities. We have shown that the thermal oxide thickness for ONO on an undiffused surface in the range 7–15 nm provides outstanding passivation. We found that a POA with nitrogen on undiffused n-type wafers is unnecessary to achieve excellent surface passivation. The field-effect passivation induced by corona charging reduced the surface recombination on most occasions, reducing it more significantly on planar {111} and rantex surfaces than on planar {100} surfaces. The deposition of charge, via corona charging can be permanently embedded within the ONO structure after annealing in FG at 400 °C and it was found to be stable after two years in ambient conditions. Finally, we demonstrated record breaking lifetimes on silicon samples featuring ONO passivation, proving this passivation scheme is amongst the best dielectric films developed, and as such, could find applications in high efficiency silicon solar cells.

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