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Letter

Transient Tap Couplers for Wafer-Level Photonic Testing Based on Optical Phase Change Materials

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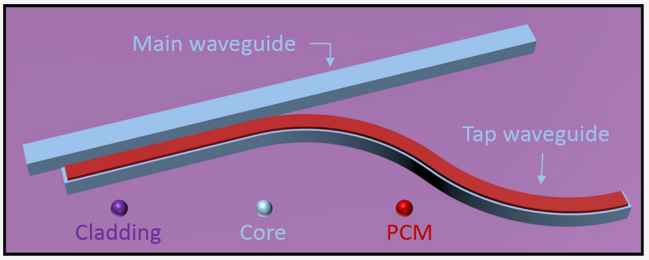
ABSTRACT: Wafer-level testing is crucial for process monitoring, post-fabrication trimming, and understanding system dynamics in photonic integrated circuits (PICs). Waveguide tap couplers are usually used to provide testing access to the PIC components. These tap couplers however incur permanent parasitic losses, imposing a trade-off between PIC performance and testing demands. Here we demonstrate a transient tap coupler design based on optical phase change materials (O-PCMs). In their as-fabricated "on" state, the couplers enable broadband interrogation of PICs at the wafer level. Upon completion of testing, the tap couplers can be turned "off" with minimal residual loss (0.01 dB) via a simple low-temperature (280 °C) wafer-scale annealing process. We further successfully demonstrated transient couplers in both Si and SiN photonics platforms. The platform-agnostic transient coupler concept uniquely combines compact footprint, broadband operation, exceptionally low residual losses, and low thermal budget commensurate with post-fabrication treatment, thereby offering a facile solution to wafer-level photonic testing without compromising the final PIC performance.



KEYWORDS: *optical phase change materials, tap couplers, photonic integrated circuits, wafer-scale testing, directional coupler, insertion loss*

Photonics integrated circuits (PICs) have witnessed tremendous strides in the past decade, opening a plethora of applications including optical communications,[1,2] sensing,[3,4] quantum optics,[5,6] and neuromorphic computing.[7,8] While individual photonic devices such as ring resonators and modulators have been studied extensively, circuit-level system engineering has become the focal point in PIC research to impart complex capabilities.[9,10] Nowadays, state-of-the-art PICs contain hundreds if not thousands of devices.[11,12] In addition to the standard input/output ports, such a complex circuit generally benefits from having multiple intermediate interrogation points to enable a subset of the circuit to be tested, for instance, to monitor the state of the optical elements during operation and post-trimming or to gain insight into the system dynamics of the circuit. Furthermore, wafer-level testing is at the heart of chip manufacturing processes, since it allows device failure to be detected in the early stage of manufacturing. Built-in test structures in PICs are essential for maximizing wafer yield and reducing production cost.[13]

Currently, wafer-level testing solutions rely on coupling a small proportion of light out from the PIC with waveguide tap couplers, which contributes to permanent total optical loss of the system.[14] PIC designers are therefore constrained by the trade-off between minimizing optical loss and ensuring adequate accessibility to testing locations. To solve this problem, various direct probing methods or erasable testing structures have been implemented.[15−18] Direct probing methods rely on evanescent or diffractive excitation of light by placing optical probes in close proximity to the waveguide surfaces.[15,16] To apply these methods, openings must be etched into the waveguide claddings to expose the waveguide core at testing sites. This technique induces excess scattering loss and might not be practical for certain PIC designs and/or packaging configurations. An alternative approach uses turning mirrors attached to the end facets of fiber or planar waveguide probes.[19,20] The approach is however limited to testing through edge couplers of PICs. Topley et al. pioneered a seminal wafer-level testing paradigm involving gratings[17] and directional couplers[18] created by germanium ion implantation in Si, which can be subsequently erased via annealing after

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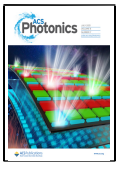

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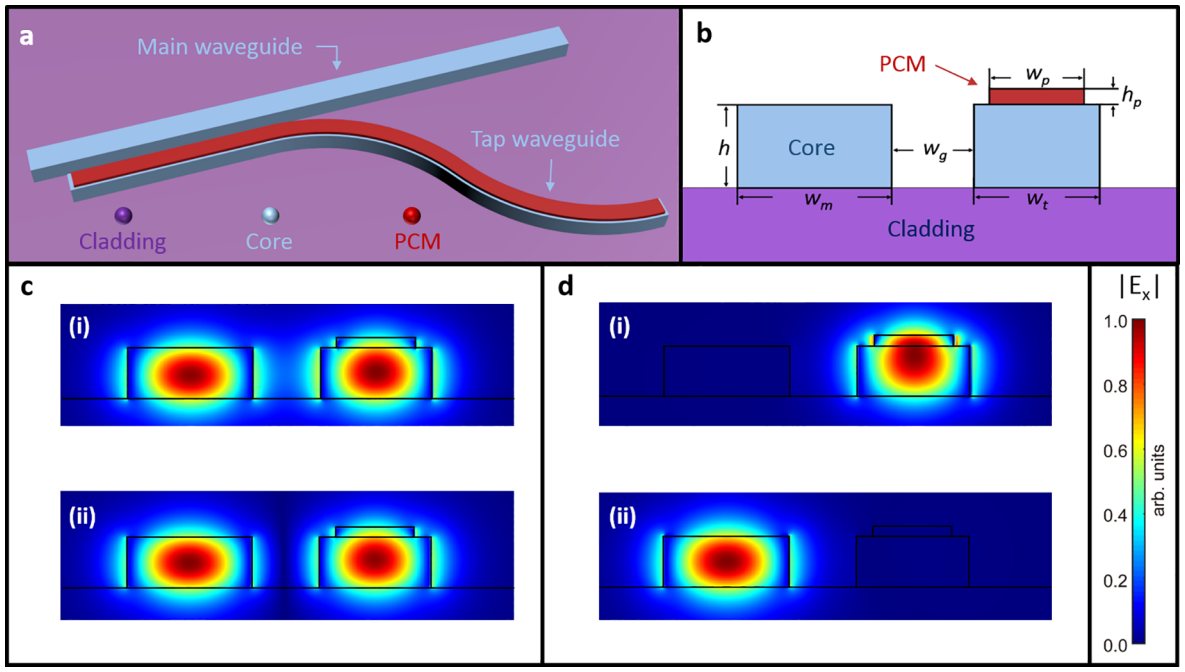

Figure 1. (a) Sketch of the transient tap coupler device. (b) Schematic device configuration of the coupling region. (c, d) Mode profiles of the coupling region when the O-PCM is at its amorphous state (c) and crystalline state (d).

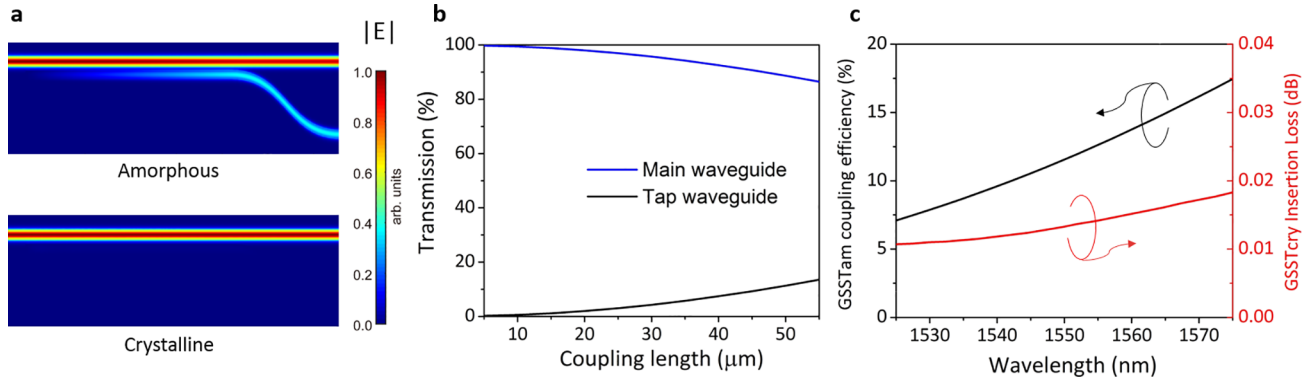

Figure 2. (a) FDTD simulation result of the electrical field magnitude profile when the O-PCM is at its amorphous state (upper) and crystalline state (lower). (b) Simulated transmission at 1550 nm in the main waveguide and tap waveguide as a function of coupling length. (c) Simulated coupling efficiency at the amorphous state and insertion loss at the crystalline state for a coupling length of 50 μm.

testing. Nonetheless, moderate loss (0.13 dB per coupler) remains after the erasure step, and the erasing process requires a high local temperature above 500 °C, mandating serial laser annealing or integrated microheaters[21] rather than wafer-scale annealing. Finally, no similar solutions are available in non-Si platforms such as SiN or III−V photonics.

In this Letter, we present a new transient coupler concept for wafer-level photonic testing. The device harnesses the large refractive index change of an optical phase change material (O-PCM), $Ge_2Sb_2Se_4Te_1$ (GSST),[22−24] during phase transition to optically modulate a directional coupler.[25,26] In its "on" state, the coupler acts as a tap to extract a fraction of optical power from the PIC. Once the testing is complete, all transient couplers on a wafer can be switched "off" using a low-temperature (280 °C) annealing process, leaving negligible (0.01 dB) residual optical loss. Since the coupler "off" state corresponds to the thermodynamically stable crystalline phase of the O-PCM, the couplers have no adverse impact on the long-term stability or performance of the PIC. Alternatively, the couplers can also be individually turned off or reactivated via local laser heating or electrothermal switching[27−30] to suit different testing needs.

DEVICE DESIGN

Our transient coupler design capitalizes on two important characteristics of chalcogenide O-PCMs to serve the wafer-level testing application. First, they exhibit a large refractive index contrast ($\Delta n > 1$) between their amorphous and crystalline states,[31] which not only facilitates a compact device architecture but also enables a "non-perturbative" design paradigm to enhance the optical contrast and lower optical loss.[23] Second, the nonvolatile nature of the material implies that the coupler is self-holding and does not necessitate power input when remaining at either the "on" or "off" state.[32] For this application, we chose GSST as the O-PCM, since it claims a large refractive index contrast ($\Delta n = 1.8$ at 1550 nm) while showing significantly reduced optical attenuation compared to the archetypal $Ge_2Sb_2Te_5$ (GST) alloy.[22] These desirable

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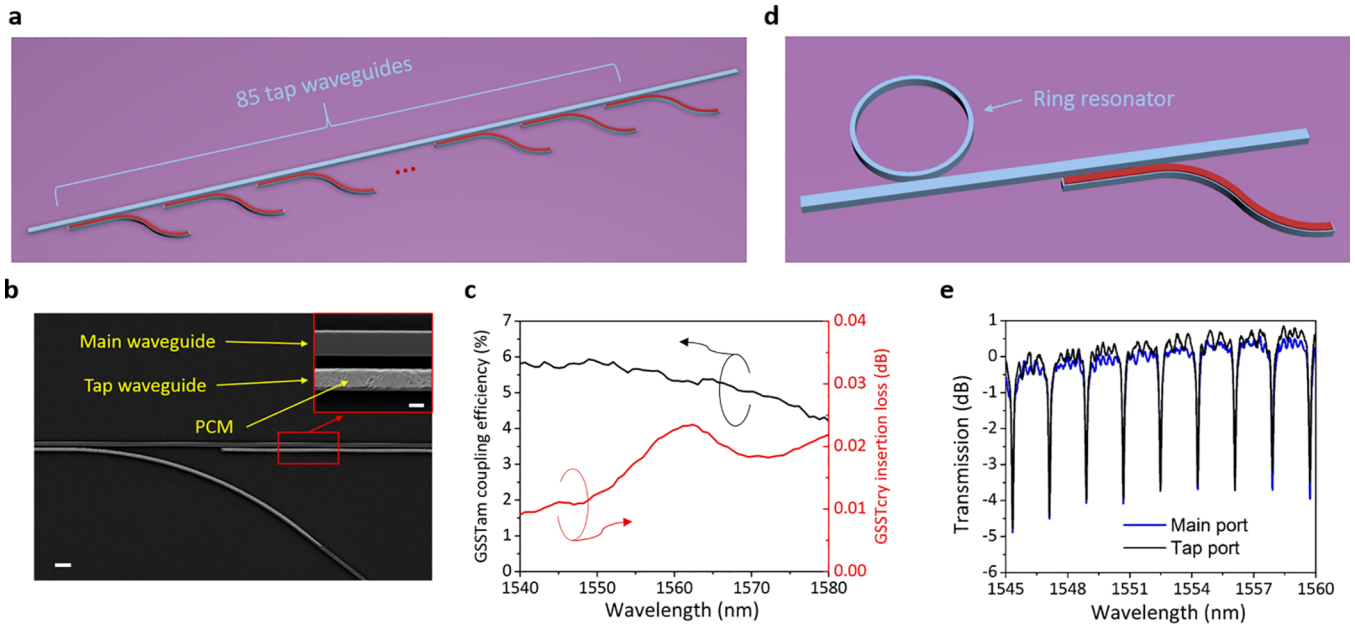

Figure 3. (a) Sketch of the device geometry for testing insertion loss when the O-PCM is at the crystalline state. (b) SEM image of the erasable directional couplers, cascaded on the main waveguide. The inset shows the zoomed-in image of the coupling region. Scale bars: 2 μm and (inset) 300 nm. (c) Measured coupling efficiency at the amorphous state and insertion loss at the crystalline state. (d) Sketch of the device geometry for validating broadband testing capability. (e) Transmission spectra at the main port and tap port after a ring resonator device. The transmission spectra are each normalized to their respective peak values.

attributes of GSST have previously been exploited in low-loss on-chip optical switch designs.[23,33−35] In addition to their excellent optical properties, chalcogenide O-PCMs are also uniquely poised for platform-agnostic integration given their amorphous structure and low processing temperatures.[36,37]

Our design of the transient coupler follows the "non-perturbative" principle. In the amorphous state, the two waveguides in the couplers are phase matched, permitting part of the light in the main PIC to be transferred to the testing waveguide. In the crystalline state, the large refractive index increase of O-PCM disrupts the phase matching condition, and hence, coupling is suppressed.

Here we validate the transient coupler design in standard silicon-on-insulator (SOI) and SiN platforms to demonstrate its versatility. The basic device geometry is depicted in Figure 1a. Each tap coupler is comprised of a "main waveguide", which is a part of a photonic circuit to be tested, and a "tap waveguide", which evanescently couples to the main waveguide to extract a fraction of light. Figure 1b illustrates the cross section of the coupling region in a transient tap coupler. The waveguides have the same core height, and their widths are optimized such that their effective indices are identical when GSST is in its amorphous state. As a result, guided modes in the two waveguides strongly hybridize, yielding well-defined even (symmetric) and odd (anti-symmetric) supermodes. The supermodes are shown in Figure 1c for an optimized SOI coupler (h = 220 nm, h_p = 40 nm, w_g = 293 nm, w_m = 552 nm, w_t = 493 nm, and w_p = 350 nm). When GSST is switched into its crystalline state, the effective index of the tap waveguide is significantly altered. The resulting index mismatch between the two waveguides leads to two isolated supermodes shown in Figure 1d.

Figure 2a presents the electrical field amplitude profile inside the SOI tap coupler in its amorphous and crystalline states, simulated using the 3-D full-vectorial finite-difference time-domain (FDTD) technique. The coupling efficiency of the device in the amorphous state can be adjusted by changing the coupling length. Figure 2b shows the optical power in the two waveguides as a function of the coupling length. When the coupling length is 50 μm, the coupling efficiency is 11% at the amorphous state. Figure 2c shows that the coupling between the two waveguides exhibits a broadband response, and thus, the device can be applied to monitor broadband spectral information. On the other hand, when GSST is crystallized, the input light remains in the main waveguide. Hence, the tap coupler is turned "off" at the crystalline state, and the minimal mode overlap with the usually more lossy crystalline O-PCM ensures low insertion loss. As shown in Figure 2c, the insertion loss remains below 0.02 dB within the entire C-band wavelength range. The switching contrast ratio, defined as the power coupling efficiency in the amorphous state over that in the crystalline state, is approximately 37.

EXPERIMENTAL RESULTS

The tap coupler devices were fabricated on an SOI substrate with a 220 nm Si layer. The waveguides were patterned via electron beam lithography, followed by reactive ion etching. The GSST patterns were fabricated on the tap waveguides via electron beam lithography and a lift-off process. GSST films were deposited via single-source thermal evaporation following our previously published protocols.[22] Stoichiometry of the GSST film was confirmed by wavelength-dispersive X-ray spectroscopy (WDS) measurements.

The devices were measured using a home-built grating coupler system in conjunction with an optical vector analyzer (LUNA Technologies OVA-5000) with a built-in external cavity tunable laser. After measuring the tap couplers in the amorphous state, the GSST-integrated devices were crystallized by an annealing process on a hot plate at 280 °C for 30 min in an inert gas atmosphere.

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In the amorphous state, coupling efficiency is calculated by normalizing the transmitted power at the tap port over the transmitted power of a single waveguide without a coupler. Experimental quantification of the residual loss in the crystalline state, on the other hand, is considerably more difficult given the very small loss. We therefore designed a test structure illustrated in Figure 3a, where 85 tap couplers couple to the same waveguide to ensure precise loss measurement. Figure 3b shows a scanning electron microscope (SEM) image of a part of the structure in Figure 3a consisting of cascaded SOI transient tap couplers. To eliminate scattering loss at waveguide junctions between GSST-coated and uncoated sections, the end of the GSST patch is inverse tapered to create a smooth transition.

Coupling efficiency at the amorphous state and insertion loss at the crystalline state for the SOI couplers are plotted in Figure 3c. The coupling efficiency stays within the range 4.3−6%, and it reaches approximately 6% at 1550 nm wavelength. The insertion loss is 0.01 dB (~0.25% loss) at 1550 nm and remains below 0.025 dB throughout the measured wavelength range. The switching contrast ratio is ~24, which is lower than the simulated value of 37 but still well sufficient to yield low residual losses.

A model structure shown in Figure 3d which comprises an SOI tap coupler placed downstream from a ring resonator was used to demonstrate operation of the tap coupler. In the amorphous state, baseline-corrected transmission spectra at the main port and the tap port are overlaid in Figure 3e. The excellent agreement between the two spectra attests to the capability of the tap coupler for broadband optical monitoring in PICs.

The transient coupler concept is similarly validated with an SiN platform. Details of the SiN device modeling and characterization outcomes are discussed in the Supporting Information. The SiN tap coupler exhibits a coupling efficiency of 20−25% in the amorphous state and a residual insertion loss of 0.09−0.13 dB (2−3% loss), corresponding to a contrast ratio of 11.7. The result indicates that the transient coupler design is generically applicable to different integrated photonics platforms.

DISCUSSION

As a vehicle to enable wafer-level testing of PICs without incurring excess loss, the transient coupler based on O-PCMs features several advantages: record low residual loss, broadband operation, small footprint, platform-agnostic integration, and versatility. Once wafer-scale testing is finished, all couplers on a wafer can be turned "off" concurrently via a single furnace annealing step at low temperatures without disrupting the performance of other on-chip devices. Alternatively, individual couplers can also be switched "on" or "off" on demand by leveraging laser or electrothermally triggered phase transition. The concept is also generic and can be adapted to other O-PCM systems besides GSST.[38,39]

To expedite adoption of the technology, one critical barrier that must be overcome is the integration of O-PCMs into the foundry process flow of PICs. Chalcogenide alloys are certainly no strangers to state-of-the-art memory foundries, which routinely employ these materials both as the information storage media and memory cell selectors.[40] As a first step toward integration of O-PCMs into standard photonic manufacturing processes, we have realized in-foundry process integration of GSST with Lincoln Laboratory's 200 mm Si and SiN integrated photonics line. Seamless integration of O-PCMs with integrated photonics will qualify the transient coupler as a promising platform for wafer-level testing.

We also note that the transient coupler represents a unique use case for O-PCMs. Since the transient coupler can be used as a one-time programmable device, many material attributes considered crucial to other applications, such as cycle lifetime, speed, and switching energy, become hardly relevant. Therefore, rational trade-offs can be made to enhance the refractive index contrast or lower the optical loss of O-PCMs for transient couplers at the expense of these traditionally valued attributes. This may open up new material design spaces for engineering of novel O-PCM alloys.

Finally, the architecture discussed herein provides a practical scheme to realize on-chip variable optical couplers, which may open up new applications in optical trimming,[41] analog optical computing,[8] on-chip optical power distribution,[42] and optical logic gates.[43]

CONCLUSION

In this Letter, a transient tap coupler notion is presented to facilitate wafer-level photonic testing. This method uses reconfigurable directional couplers based on optical phase change materials to extract light at intermediate interrogation points in a photonic circuit. A subsequent wafer-scale, low-temperature furnace annealing step optically switches off the couplers to prevent permanent loss penalty. A record low residual loss of 0.01 dB is experimentally validated at 1550 nm wavelength. The proposed coupler design further features broadband response and a small footprint and is compatible with integration into different integrated photonics platforms such as Si and SiN. This testing platform offers a facile route for integrated photonics manufacturing quality control and post-production monitoring of large-scale photonic circuits.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.1c00374.

Optical constants of GSST, transient tap coupler in a SiN photonic platform, and tolerance study of the transient tap coupler (PDF)

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Cheng, Q.; Rumley, S.; Bahadori, M.; Bergman, K. Photonic Switching in High Performance Datacenters [Invited]. *Opt. Express* **2018**, *26* (12), 16022.

(2) Spencer, D. T.; Lee, S. H.; Oh, D. Y.; Suh, M.-G.; Yang, K. Y.; Vahala, K. An Optical-Frequency Synthesizer Using Integrated Photonics. *Nature* **2018**, *557* (7703), 81−85.

(3) Kita, D. M.; Miranda, B.; Favela, D.; Bono, D.; Michon, J.; Lin, H.; Gu, T.; Hu, J. High-Performance and Scalable on-Chip Digital Fourier Transform Spectroscopy. *Nat. Commun.* **2018**, *9* (1), 1−7.

(4) García-Meca, C.; Lechago, S.; Brimont, A.; Griol, A.; Mas, S.; Sánchez, L.; Bellieres, L.; Losilla, N. S.; Martí, J. On-Chip Wireless Silicon Photonics: From Reconfigurable Interconnects to Lab-on-Chip Devices. *Light: Sci. Appl.* **2017**, *6* (9), No. e17053.

(5) Harris, N. C.; Steinbrecher, G. R.; Prabhu, M.; Lahini, Y.; Mower, J.; Bunandar, D.; Chen, C.; Wong, F. N. C.; Baehr-Jones, T.; Hochberg, M.; Lloyd, S.; Englund, D. Quantum Transport Simulations in a Programmable Nanophotonic Processor. *Nat. Photonics* **2017**, *11* (7), 447−452.

(6) Dyakonov, I. V.; Pogorelov, I. A.; Bobrov, I. B.; Kalinkin, A. A.; Straupe, S. S.; Kulik, S. P.; Dyakonov, P. V.; Evlashin, S. A. Reconfigurable Photonics on a Glass Chip. *Phys. Rev. Appl.* **2018**, *10* (4), 1.

(7) Feldmann, J.; Youngblood, N.; Wright, C. D.; Bhaskaran, H.; Pernice, W. H. P. All-Optical Spiking Neurosynaptic Networks with Self-Learning Capabilities. *Nature* **2019**, *569* (7755), 208−214.

(8) Shen, Y.; Harris, N. C.; Skirlo, S.; Prabhu, M.; Baehr-Jones, T.; Hochberg, M.; Sun, X.; Zhao, S.; Larochelle, H.; Englund, D.; Soljacic, M. Deep Learning with Coherent Nanophotonic Circuits. *Nat. Photonics* **2017**, *11* (7), 441−446.

(9) Bogaerts, W.; Pérez, D.; Capmany, J.; Miller, D. A. B.; Poon, J.; Englund, D.; Morichetti, F.; Melloni, A. Programmable Photonic Circuits. *Nature* **2020**, *586* (7828), 207−216.

(10) Bogaerts, W.; Rahim, A. Programmable Photonics: An Opportunity for an Accessible Large-Volume PIC Ecosystem. *IEEE J. Sel. Top. Quantum Electron.* **2020**, *26* (5), 1−17.

(11) Sun, J.; Timurdogan, E.; Yaacobi, A.; Hosseini, E. S.; Watts, M. R. Large-Scale Nanophotonic Phased Array. *Nature* **2013**, *493*, 195.

(12) Seok, T. J.; Kwon, K.; Henriksson, J.; Luo, J.; Wu, M. C. Wafer-Scale Silicon Photonic Switches beyond Die Size Limit. *Optica* **2019**, *6* (4), 490.

(13) Baehr-Jones, T.; Pinguet, T.; Lo Guo-Qiang, P.; Danziger, S.; Prather, D.; Hochberg, M. Myths and Rumours of Silicon Photonics. *Nat. Photonics* **2012**, *6* (4), 206−208.

(14) Polster, R.; Dai, L. Y.; Cheng, Q.; Oikonomou, M.; Rumley, S.; Bergman, K. Challenges and Solutions for High-Volume Testing of Silicon Photonics. *Silicon Photonics XIII* **2018**, *10537*, 1053703.

(15) Scheerlinck, S.; Taillaert, D.; Van Thourhout, D.; Baets, R. Flexible Metal Grating Based Optical Fiber Probe for Photonic Integrated Circuits. *Appl. Phys. Lett.* **2008**, *92* (3), 031104.

(16) Michels, T.; Aksyuk, V. Optical Probe for Nondestructive Wafer-Scale Characterization of Photonic Elements. *IEEE Photonics Technol. Lett.* **2017**, *29* (8), 643−646.

(17) Topley, R.; Martinez-Jimenez, G.; Ofaolain, L.; Healy, N.; Mailis, S.; Thomson, D. J.; Gardes, F. Y.; Peacock, A. C.; Payne, D. N. R.; Mashanovich, G. Z.; Reed, G. T. Locally Erasable Couplers for Optical Device Testing in Silicon on Insulator. *J. Lightwave Technol.* **2014**, *32* (12), 2248−2253.

(18) Chen, X.; Milosevic, M. M.; Runge, A. F. J.; Yu, X.; Khokhar, A. Z.; Mailis, S.; Thomson, D. J.; Peacock, A. C.; Saito, S.; Reed, G. T. Silicon Erasable Waveguides and Directional Couplers by Germanium Ion Implantation for Configurable Photonic Circuits. *Opt. Express* **2020**, *28* (12), 17630.

(19) Polster, R.; Dai, L. Y.; Jimenez, O. A.; Cheng, Q.; Lipson, M.; Bergman, K. Wafer-Scale High-Density Edge Coupling for High Throughput Testing of Silicon Photonics. *2018 Opt. Fiber Commun. Conf. Expo. OFC 2018 - Proc.* 2018, 1−3.

(20) Trappen, M.; Blaicher, M.; Dietrich, P.-I.; Dankwart, C.; Xu, Y.; Hoose, T.; Billah, M. R.; Abbasi, A.; Baets, R.; Troppenz, U.; Theurer, M.; Wörhoff, K.; Seyfried, M.; Freude, W.; Koos, C. 3D-Printed Optical Probes for Wafer-Level Testing of Photonic Integrated Circuits. *Opt. Express* **2020**, *28* (25), 37996.

(21) Yu, X.; Chen, X.; Milosevic, M. M.; Yan, X.; Saito, S.; Reed, G. T. Electrically Erasable Optical I/O for Wafer Scale Testing of Silicon Photonic Integrated Circuits. *IEEE Photonics J.* **2020**, *12* (5), 1−8.
(22) Zhang, Y.; Chou, J. B.; Li, J.; Li, H.; Du, Q.; Yadav, A.; Zhou, S.; Shalaginov, M. Y.; Fang, Z.; Zhong, H.; Roberts, C.; Robinson, P.; Bohlin, B.; Ríos, C.; Lin, H.; Kang, M.; Gu, T.; Warner, J.; Liberman, V.; Richardson, K.; Hu, J. Broadband Transparent Optical Phase Change Materials for High-Performance Nonvolatile Photonics. *Nat. Commun.* **2019**, *10* (1), 4279.
(23) Zhang, Q.; Zhang, Y.; Li, J.; Soref, R.; Gu, T.; Hu, J. Broadband Nonvolatile Photonic Switching Based on Optical Phase Change Materials: Beyond the Classical Figure-of-Merit. *Opt. Lett.* **2018**, *43* (1), 94.
(24) Zhang, Y.; Li, J.; Chou, J. B.; Fang, Z.; Yadav, A.; Lin, H.; Du, Q.; Michon, J.; Han, Z.; Huang, Y.; Zheng, H.; Gu, T.; Liberman, V.; Richardson, K.; Hu, J. Broadband Transparent Optical Phase Change Materials. In *Optics InfoBase Conference Papers*; 2017; Vol. Part F43-C. DOI: 10.1364/CLEO_AT.2017.JTh5C.4.
(25) Xu, P.; Zheng, J.; Doylend, J. K.; Majumdar, A. Low-Loss and Broadband Nonvolatile Phase-Change Directional Coupler Switches. *ACS Photonics* **2019**, *6* (2), 553−557.
(26) Ikuma, Y.; Saiki, T.; Tsuda, H. Proposal of a Small Self-Holding 2 × 2 Optical Switch Using Phase-Change Material. *IEICE Electron. Express* **2008**, *5* (12), 442−445.
(27) Zhang, Y.; Fowler, C.; Liang, J.; Azhar, B.; Shalaginov, M. Y.; An, S.; Hu, J. Electrically Reconfigurable Nonvolatile Metasurface Using Low-Loss Optical Phase Change Material. *Nat. Nanotechnol.* **2021**, *16*, 661.
(28) Zheng, J.; Fang, Z.; Wu, C.; Zhu, S.; Xu, P.; Doylend, J. K.; Deshmukh, S.; Pop, E.; Dunham, S.; Li, M.; Majumdar, A. Nonvolatile Electrically Reconfigurable Integrated Photonic Switch Enabled by a Silicon PIN Diode Heater. *Adv. Mater.* **2020**, *32*, 2001218.
(29) Zhang, H.; Zhou, L.; Lu, L.; Xu, J.; Wang, N.; Hu, H.; Rahman, B. M. A.; Zhou, Z.; Chen, J. Miniature Multilevel Optical Memristive Switch Using Phase Change Material. *ACS Photonics* **2019**, *6* (9), 2205−2212.
(30) Ríos, C.; Zhang, Y.; Shalaginov, M.; Deckoff-Jones, S.; Wang, H.; An, S.; Zhang, H.; Kang, M.; Richardson, K. A.; Roberts, C.; Chou, J.; Liberman, V.; Vitale, S. A.; Kong, J.; Gu, T.; Hu, J. Multi-Level Electro-Thermal Switching of Optical Phase-Change Materials Using Graphene. *Adv. Photonics Res.* **2021**, *2* (1), 2000034.
(31) Kooi, B. J.; Wuttig, M. Chalcogenides by Design: Functionality through Metavalent Bonding and Confinement. *Adv. Mater.* **2020**, *32* (21), 1908302.
(32) Wuttig, M.; Bhaskaran, H.; Taubner, T. Phase-Change Materials for Non-Volatile Photonic Applications. *Nat. Photonics* **2017**, *11* (8), 465−476.
(33) Jiang, W. Nonvolatile and Ultra-Low-Loss Reconfigurable Mode (De)Multiplexer/Switch Using Triple-Waveguide Coupler with Ge2Sb2Se4Te1 Phase Change Material. *Sci. Rep.* **2018**, *8* (1), 1−12.
(34) De Leonardis, F.; Soref, R.; Passaro, V. M. N.; Zhang, Y.; Hu, J. Broadband Electro-Optical Crossbar Switches Using Low-Loss Ge2Sb2Se4Te1 Phase Change Material. *J. Lightwave Technol.* **2019**, *37* (13), 3183.
(35) Dhingra, N.; Song, J.; Saxena, G. J.; Sharma, E. K.; Rahman, B. M. A. Design of a Compact Low-Loss Phase Shifter Based on Optical Phase Change Material. *IEEE Photonics Technol. Lett.* **2019**, *31* (21), 1757−1760.
(36) Zou, Y.; Moreel, L.; Lin, H.; Zhou, J.; Li, L.; Danto, S.; Musgraves, J. D.; Koontz, E.; Richardson, K.; Dobson, K. D.; Birkmire, R.; Hu, J. Solution Processing and Resist-Free Nanoimprint Fabrication of Thin Film Chalcogenide Glass Devices: Inorganic-Organic Hybrid Photonic Integration. *Adv. Opt. Mater.* **2014**, *2* (8), 759−764.
(37) Hu, J.; Li, L.; Lin, H.; Zou, Y.; Du, Q.; Smith, C.; Novak, S.; Richardson, K.; Musgraves, J. D. Chalcogenide Glass Microphotonics: Stepping into the Spotlight. *Am. Ceram. Soc. Bull.* **2015**, *94* (4), 24−29.
(38) Dong, W.; Liu, H.; Behera, J. K.; Lu, L.; Ng, R. J. H.; Sreekanth, K. V.; Zhou, X.; Yang, J. K. W.; Simpson, R. E. Wide Bandgap Phase Change Material Tuned Visible Photonics. *Adv. Funct. Mater.* **2019**, *29* (6), 1806181.
(39) Delaney, M.; Zeimpekis, I.; Lawson, D.; Hewak, D. W.; Muskens, O. L. A New Family of Ultralow Loss Reversible Phase-Change Materials for Photonic Integrated Circuits: Sb2S3 and Sb2Se3. *Adv. Funct. Mater.* **2020**, *30* (36), 2002447.
(40) Cheng, H. Y.; Chien, W. C.; Kuo, I. T.; Lai, E. K.; Zhu, Y.; Jordan-Sweet, J. L.; Ray, A.; Carta, F.; Lee, F. M.; Tseng, P. H.; Lee, M. H.; Lin, Y. Y.; Kim, W.; Bruce, R.; Yeh, C. W.; Yang, C. H.; Brightsky, M.; Lung, H. L. An Ultra High Endurance and Thermally Stable Selector Based on TeAsGeSiSe Chalcogenides Compatible with BEOL IC Integration for Cross-Point PCM. *Technol. Dig. - Int. Electron Devices Meet. IEDM* **2018**, *2*, 2.2.1−2.2.4.
(41) Miller, D. A. B. Perfect Optics with Imperfect Components. *Optica* **2015**, *2* (8), 747.
(42) Thapliya, R.; Kikuchi, T.; Nakamura, S. Tunable Power Splitter Based on an Electro-Optic Multimode Interference Device. *Appl. Opt.* **2007**, *46* (19), 4155−4161.
(43) Fujisawa, T.; Koshiba, M. All-Optical Logic Gates Based on Nonlinear Slot-Waveguide Couplers. *J. Opt. Soc. Am. B* **2006**, *23* (4), 684.

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