



Process–Structure–Properties Relationships of Passivating, Electron-Selective Contacts Formed by Atmospheric Pressure Chemical Vapor Deposition of Phosphorus-Doped Polysilicon

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Herein, we investigate the process–structure–properties relationships of in situ phosphorus (P)-doped polycrystalline silicon (poly-Si) films by atmospheric pressure chemical vapor deposition (APCVD) for fabricating poly-Si passivating, electron selective contacts. This high-throughput in-line APCVD technique enables to achieve a low-cost, simple manufacturing process for crystalline silicon (c-Si) solar cells featuring poly-Si passivating contact by excluding the need for vacuum/plasma environment, and additional post-deposition doping steps. A thin layer of this P-doped poly-Si is deposited on an ultrathin (1.5 nm) silicon oxide (SiO_x) coated c-Si substrate to fabricate the passivating contact. This is followed by various post-deposition treatments, including a high-temperature annealing step and hydrogenation process. The poly-Si films are characterized to achieve a better understanding of the impacts of deposition process conditions and post-deposition treatments on the microstructure, electrical conductivity, passivation quality, and carrier selectivity of the contacts which assists to identify the optimal process conditions. In this work, the optimized annealing process with post-hydrogenation yields passivating contact with a saturation current density (J_0) of 3 fA cm^{-2} and an implied open-circuit voltage (iV_{OC}) of 712 mV on planar c-Si wafer. Junction resistivity values ranging from 50 to $260 \text{ m}\Omega \text{ cm}^2$ are realized for the poly-Si contacts processed in the optimal annealing condition.

1. Introduction

With the advancement of crystalline silicon (c-Si) photovoltaics (PV), passivating contacts have become a necessary part of the highest efficiency c-Si PV cells. A passivating, carrier-selective layer extracts carriers from the absorber efficiently by passivating interface defects and providing selectivity to the majority carriers.^[1,2] The key to this contact technology is reducing recombination losses without increasing resistive losses. The passivating, carrier-selective functionality can be achieved using different materials systems, such as the stack of ultrathin dielectric layers including silicon oxide (SiO_x),^[3] aluminum oxide (Al_2O_3),^[4–6] various transition metal oxides,^[3,5–8] and a stack of hydrogenated doped and undoped amorphous silicon (a-Si:H) layers.^[9,10] Another effective approach is to use a very thin SiO_x layer with a heavily doped polycrystalline silicon (poly-Si) layer, also known as a tunnel oxide passivated poly-Si contact (TOPCon)^[11–16] or poly-Si on oxide (POLO).^[17–19]

The high efficiencies obtained with oxide-passivated poly-Si contacts are due to the excellent passivation quality and carrier selectivity. Moving forward, the development of a fabrication

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DOI: 10.1002/pssr.202100639

process that is simple, cost-effective, and compatible with mass production is essential to implement this contact technology in industrial solar cell production. Atmospheric pressure chemical vapor deposition (APCVD) is a single side deposition process with high throughput that is operated in atmospheric pressure conditions. This process is cost-effective and simple as it does not require any low pressure/vacuum environment or plasma processes like other traditionally used deposition processes, such as low-pressure chemical vapor deposition (LPCVD),^[12,18,20,21] and plasma-enhanced chemical vapor deposition (PECVD).^[13,15,22] Also, the deposition rate in the APCVD process is significantly higher than the deposition rate in LPCVD and PECVD.^[23] Moreover, in situ phosphorus (P) doped silicon (Si) films are grown with this APCVD process and therefore excludes the additional ex situ doping steps used in many other works.

A high-quality passivating, electron-selective contact fabricated using APCVD in situ P-doped poly-Si film and thin thermally grown SiO_x layer was reported in a previous study.^[24] In this work, we present a passivating electron-selective contact fabricated with APCVD in situ P-doped poly-Si layer on top of a thin SiO_x layer grown using deionized water with dissolved ozone (DI-O₃).^[4,25] Additionally, the influence of the deposition process and annealing process parameters on the microstructure, electrical properties, and passivation quality of the contact is reported, providing guidance on the optimal fabrication process for the APCVD-based poly-Si electron contacts. Finally, by the better understanding of the process–structure–properties relationship of the contact, we can achieve even lower saturation current density (*J*₀) and junction resistivity compared to the previous work.^[24]

2. Results and Discussion

2.1. Composition, Microstructure, and Electrical Properties of the APCVD Poly-Si Thin Films

The deposition temperatures and PH₃ ratios listed in **Table 1** were used to deposit the P-doped Si films yielding deposition rates of around 11–14 nm s⁻¹, significantly higher than the PECVD and LPCVD processes.^[23] **Figure 1a–c** shows the X-ray diffraction (XRD) spectra of the APCVD P-doped Si films in as-deposited and annealed conditions.

From **Figure 1a**, we can see that the doped Si layers deposited at a lower temperature (695 °C) are mostly amorphous after deposition as the XRD spectra show no peaks for the crystalline phase. This is also demonstrated by the Raman spectra of the as-deposited samples in **Figure 1d**. The films deposited at 695 °C show a large shoulder at 480 cm⁻¹ attributed to an amorphous phase.^[26] There appears to be the presence of Si nanocrystals in

Table 1. Deposition zone temperature and PH₃ ratio used for the Si layer depositions.

Batch	PH ₃ gas ratio [%]	Deposition zone temperature, <i>T</i> _d [°C]
A	1.48	695
B	4.00	695
C	9.09	695
D	1.48	750
E	4.00	750
F	9.09	750

the amorphous matrix based on the small peak observed at around 518 cm⁻¹. The peak at 518 cm⁻¹ for the sample with the highest PH₃ ratio (9.09%) is smaller than the sample with the lower PH₃ ratio (1.48%). This indicates a lower concentration of nanocrystals in the film with a higher PH₃ ratio.

At the higher deposition temperature (750 °C), the resulting as-deposited films are polycrystalline according to both the Raman and XRD spectra. These samples feature a sharp peak for crystalline Si at 520 cm⁻¹ (**Figure 1d**).^[26] The asymmetry in the peak at 520 cm⁻¹ is caused by the presence of nanocrystals and electrically active dopants (i.e., P).^[27] The XRD spectra of these samples show diffraction peaks at 2θ values of around 28.5°, 47.5°, and 56.3°. These three diffraction peaks are for {111}, {220}, and {311} Si crystal planes. The diffraction peaks get broader with increasing of PH₃ gas ratio indicating a higher degree of crystallinity in the Si films with a lower P concentration.

As expected, the SIMS data in **Figure 2a** shows the average P concentration in the Si films increases with the PH₃ ratio. For the PH₃ ratio of 1.48%, the Si film deposited at 750 °C has a higher P concentration than the sample deposited at 695 °C. In contrast, for PH₃ ratios of 4.00% and 9.09%, the films deposited at 695 °C have a higher P concentration. P concentration of the films deposited with 4.00% and 9.09% PH₃ ratios are above the solid solubility limit of Si for the annealing temperatures of 850 °C and 900 °C used in this work.^[28] This suggests that all the P atoms do not create electrically active carriers after the annealing process.

All the batches were fully crystallized after annealing at 850 °C and 900 °C, as demonstrated by a sharp peak at 520 cm⁻¹ and the absence of the shoulder at around 480 cm⁻¹ for the amorphous phase in the Raman spectra (see supporting information S1 and S2). **Figure 1b,c** shows the XRD spectra of the poly-Si layers annealed at *T*_a = 850 °C for 30 min and *T*_a = 900 °C for 20 minutes, respectively. All the XRD spectra show peaks for {111}, {220}, and {311} crystal planes, including the samples deposited at 695 °C that did not show these sharp diffraction peaks prior to annealing. The samples deposited at 750 °C were already polycrystalline before annealing and no significant

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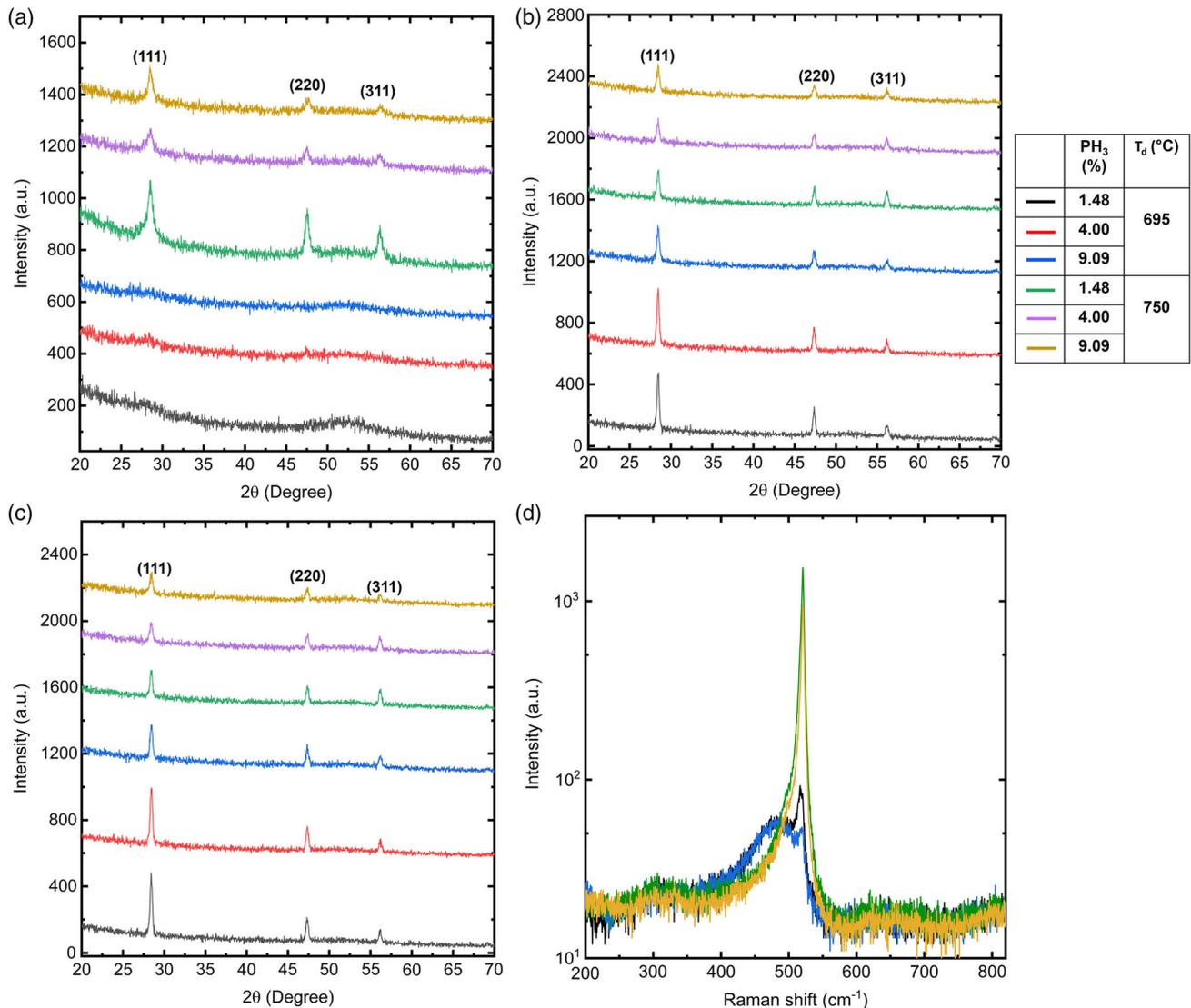


Figure 1. GI-XRD spectra of the APCVD doped Si layers in: a) the as-deposited state; b) after annealing at 850 °C for 30 min; and c) after annealing at 900 °C for 20 min. d) Raman spectra of the as-deposited APCVD Si films.

change is observed in the XRD spectra of these samples following annealing.

The crystallite size of the annealed poly-Si films was determined from the XRD peaks using the Scherrer formula.^[29] The change in the grain size and the phase transition of the APCVD Si films before and after annealing were also evaluated with atomic force microscopy (AFM) measurements (see S3 and S4, Supporting Information). It is evident from both the XRD spectra and AFM images of the samples that the crystallinity and grain size of the Si films are controlled not only by the deposition temperature but also by the P concentration. **Figure 3b** shows that with the increase of P concentration, crystallite size decreases in both low-deposition and high-deposition temperature batches. This suggests that low P concentration leads to the reduction of nuclei formation rate during solid-phase crystallization which facilitates grain growth.^[30]

In contrast, higher P concentration not only enhances the nucleation rate but also hinders the grain growth by segregating on the grain boundaries.^[31] The intensity of the peak for {111} plane is higher than the other two peak intensities for the batches deposited at low temperature (695 °C) and using a low PH₃ ratio (1.48% and 4.00%) (Figure 1b,c). This refers to the preferential orientation of the crystallites/grains along <111> direction.^[32] But the ratio of the {111} peak intensity to the intensity of the peaks for {220} and {311} crystal planes decreases with the increase of the phosphorus concentration and the deposition temperature (Figure 1b,c). This suggests that the doped poly-Si layers deposited at 750 °C (crystalline in as-deposited condition) and with higher P concentration (9.09% PH₃) have comparatively smaller crystallites/grains without any preferential orientation. The microstructure and the dopant concentration have a significant influence on the electrical properties of the

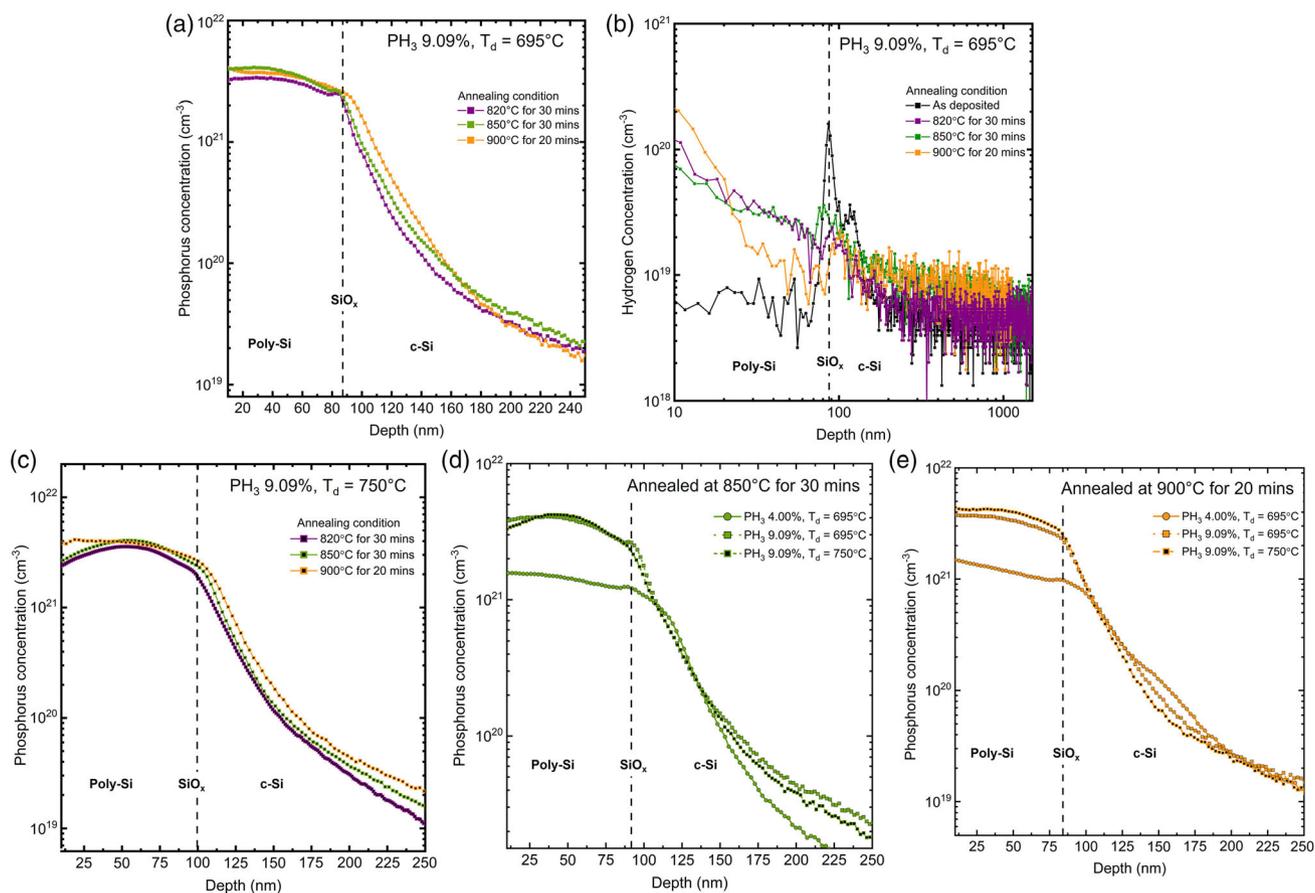


Figure 2. a) Phosphorus and b) hydrogen depth profiles of the samples deposited at 695 °C using a 9.09% PH₃ gas ratio. c) Phosphorus depth profiles of the samples deposited at 750 °C using a 9.09% PH₃ gas ratio. Phosphorus depth profiles of multiple samples annealed at d) 850 °C for 30 min and e) 900 °C for 20 min.

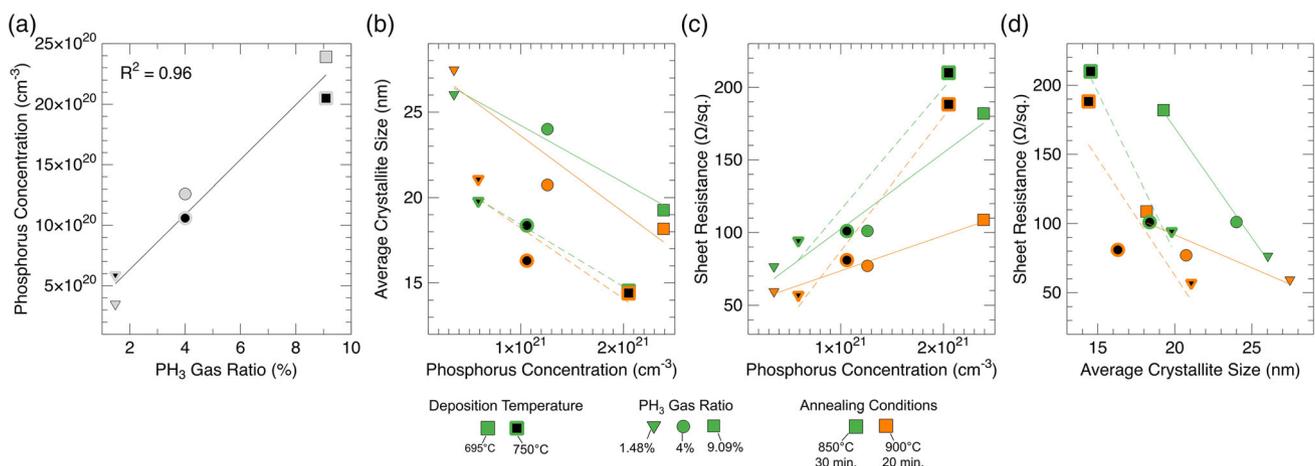


Figure 3. a) Average P concentrations in the as-deposited APCVD silicon films versus the PH₃ gas ratio at both deposition temperatures. b) Crystallite size versus P concentration in the poly-Si films after annealing. c) Sheet resistance of the poly-Si films versus P concentration of the poly-Si. d) Sheet resistance of the poly-Si films versus crystallite size.

doped Si layer. Figure 3c shows the sheet resistance of all the batches after annealing at 850 °C and 900 °C. We can see that sheet resistance of the annealed poly-Si layer increases with

the increase of the P concentration. Besides that, the batches deposited at 750 °C have higher sheet resistance than their corresponding batches deposited at low temperature.

The sheet resistance of the doped poly-Si layer depends on the crystallinity, grain size, active carrier concentrations, film thickness, and dopant diffusion depth in the c-Si. In this work, poly-Si film thicknesses were kept identical in all the batches. But there is a variation in dopant concentration, dopant diffusion, and microstructure of the poly-Si films. Grain/crystallite size reduction has been observed with the increase of the P concentration and the deposition temperature (Figure 3b). From Figure 3c,d, we can see that sheet resistance increases with the increase of P concentration and the decrease of crystallite size. Carrier trapping and scattering by grain boundaries lower the mobility of the active carriers.^[33,34] Besides that, with the increase of the active carrier concentration in the poly-Si film, carrier mobility decreases due to the enhanced carrier scattering.^[35,36] Hence, poly-Si layers with higher P concentrations have lower carrier mobilities. This phenomenon was also observed in another work on in situ P-doped poly-Si by Meriç Firat et al.

Low carrier mobility causes less dopant diffusion into the c-Si through the SiO_x layer, which also elevates the sheet resistance of the poly-Si/SiO_x contact. Besides that, a higher amount of P segregated as the electrically inactive P on the grain boundaries in the heavily doped poly-Si film with smaller crystallite size and higher number of grain boundaries.^[34,37] Therefore, comparatively higher sheet resistance has been observed for the poly-Si layer with high P concentration and fine-grain microstructure.

Figure 3c demonstrates the reduction of the sheet resistance with the increase of annealing temperature. This is because of the elevation of crystallinity and active carrier concentrations in the poly-Si films due to the high-temperature annealing process. Additionally, higher annealing temperature results in more dopant diffusion into the c-Si (Figure 2a,c), which also lowers the sheet resistance of poly-Si contact. From Figure 2a, we can see the phosphorus spike at the poly-Si/SiO_x interface when annealed at 820 and 850 °C which is not observed in the case of 900 °C. This is due to the higher amount of dopant diffusion into the absorber at 900 °C annealing also reported by other work.^[38]

2.2. Surface Passivation Quality

In the as-deposited condition, all the batches demonstrate very high saturation current density (J_0) and very low implied open-circuit voltage (iV_{OC}). Therefore, the samples were annealed for passivation activation. Excellent surface passivation quality of poly-Si contacts is achieved by the combination of a few mechanisms: 1) chemical passivation by the interfacial SiO_x (tunnel oxide) layer and the atomic hydrogen at the interface^[39]; and 2) field-effect passivation induced by the band bending at the c-Si interface.^[40] Band bending at the c-Si interface is induced by the active dopants in the poly-Si layer and the shallow diffused region in the c-Si.^[12,40] The shallow dopant diffusion into the c-Si not only improves the surface passivation quality by enhancing field-effect passivation, but also reduces the contact resistivity. However, excessive dopant diffusion into the c-Si degrades the surface passivation quality by increasing Auger recombination.^[41]

The ultrathin SiO_x layer not only provides chemical passivation but also acts as a dopant diffusion barrier and restricts excessive dopant diffusion into the c-Si absorber. This helps keep the P concentration in the poly-Si layer high enough to provide strong field-effect passivation. The electrically inactive P segregates at the grain boundaries and piles up at the poly-Si/SiO_x interface, helping passivate the defects at these sites.^[21,42] This SiO_x layer also helps to reduce Auger recombination by restricting excessive dopant diffusion. All of these above-mentioned mechanisms are behind the excellent passivating carrier selective functionality of poly-Si contacts.

Figure 4a,b demonstrates the average J_0 and iV_{OC} of the APCVD poly-Si samples after the high-temperature annealing. Surface passivation of the poly-Si contact starts to improve with the annealing process. Annealing at 820 °C reduces the J_0 value and improves the iV_{OC} of the contact. Comparatively lower J_0 and higher iV_{OC} have been observed for the batches with higher P concentration after annealing at 820 °C for 30 min as low P concentration in poly-Si layer results in low field-effect passivation at the interface.^[12] Passivation quality keeps improving with the increase of annealing temperature up to 850 °C. Figure 4a shows

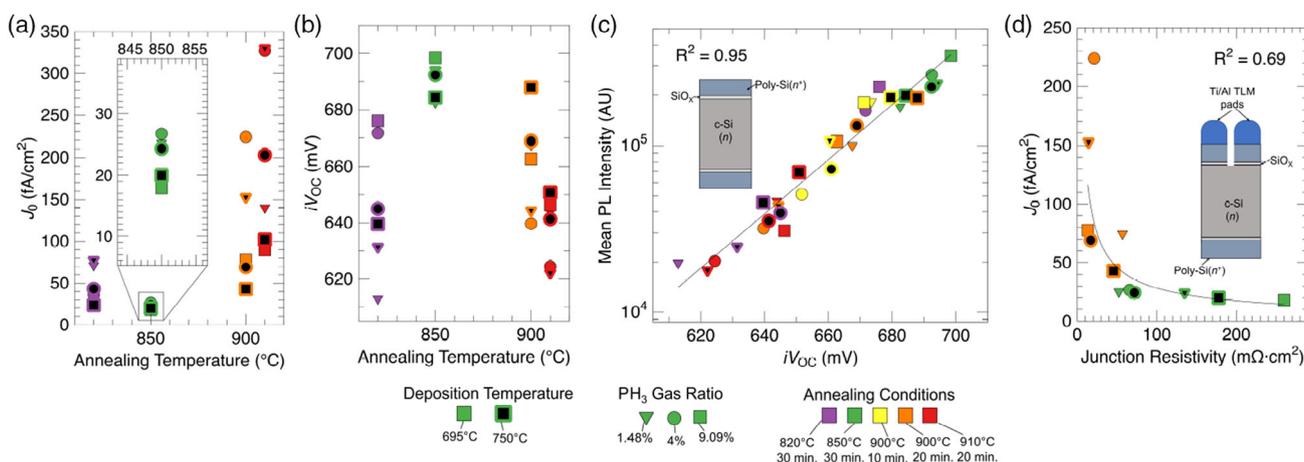


Figure 4. a) Saturation current density (J_0) of the poly-Si samples for different annealing conditions. b) Implied open-circuit voltage (iV_{OC}) of the poly-Si samples for different annealing conditions. c) Mean photoluminescence (PL) intensity versus iV_{OC} of the symmetrical samples annealed for different conditions on a log-linear plot. d) J_0 versus junction resistivity of the poly-Si contacts annealed at 850 and 900 °C.

that the J_0 values of all the batches reach their lowest values when annealed at 850 °C for 30 min. This annealing condition also resulted in the highest iV_{OC} for all the batches except for the batch deposited at 750 °C with 9.09% PH₃ ratio. The excellent surface passivation at 850 °C originates from the enhancement of the chemical passivation and the field-effect passivation. Chemical passivation improvement emerges from the reorientation of the SiO_x bonding at the interface at this temperature.^[39] Moreover, increased active dopant concentration in the poly-Si layer and dopant diffusion (Figure 2a) through the SiO_x layer into the c-Si increase the band bending at the interface^[24] and thus enhance the field-effect passivation. The combination of these mechanisms provides this excellent surface passivation after annealing at 850 °C for 30 min. The batches annealed at 850 °C show a similar trend as the batches annealed at 820 °C with respect to the J_0 and iV_{OC} values. The poly-Si layer with higher P concentration demonstrates the lower J_0 . The lowest J_0 and the highest iV_{OC} have been achieved for the poly-Si batch deposited at 695 °C with a 9.09% PH₃ ratio. J_0 as low as 13 fA cm⁻² and iV_{OC} as high as 701 mV have been achieved for this batch without any hydrogenation process.

Raising the annealing temperature above 850 °C increases the J_0 and lowers the iV_{OC} (Figure 4a,b). This is because of the excessive dopant diffusion into the c-Si due to the high annealing temperature which increases the Auger recombination. Figure 2a,c,e shows a higher amount of dopant diffusion into the c-Si during 900 °C annealing. Moreover, other studies have shown pinholes and damage formation in the SiO_x layer when annealed at this high temperature which degrades the chemical passivation.^[43–45] In addition, hydrogen at the poly-Si/SiO_x interface effuses out during the annealing process (Figure 2b), which deteriorates the chemical passivation of the interface.

Though the J_0 value of the batch deposited at 750 °C with a 9.09% PH₃ ratio increases after annealing at 900 °C, iV_{OC} also increases and reaches its maximum value. Besides that, the increase in J_0 is not as steep as the J_0 increment observed for other batches. This is because of its small crystallite size and lower carrier mobility of the poly-Si layer, which causes lower P diffusion into the c-Si during annealing. For this batch, increasing of annealing temperature to 900 °C causes more dopant diffusion into the c-Si which enhances the field-effect passivation and the iV_{OC} . But the dopant diffusion is not as excessive as the dopant diffusion in other batches to increase the Auger recombination significantly. Figure 2e demonstrates that the dopant diffusion in this batch is lower than the dopant diffusion in the batches deposited at 695 °C with a 4.00% PH₃ ratio when annealed at 900 °C.

In contrast, poly-Si contact deposited at 695 °C with a 4.00% PH₃ ratio shows very high dopant diffusion into the c-Si (Figure 2e), which explains the significant increase in J_0 of this batch when annealed at 900 °C (Figure 4a). Dopant diffusion into the c-Si depends on the concentration and the mobility of the dopant in the doped poly-Si. The dopant diffusion into the c-Si for heavily doped poly-Si with lower dopant mobility is less than the dopant diffusion for the moderately doped batch with higher dopant mobility. This is also supported by the sheet resistance value of the poly-Si layers (Figure 3c,d). The sheet resistance of the batches deposited with a 9.09% PH₃ ratio is higher than the sheet resistance of the batches with a 4.00%

PH₃ ratio, which refers to less dopant diffusion for the batches with higher P concentration.

Annealing at 910 °C increases the J_0 more and consequently, lowers the iV_{OC} of all the batches (Figure 4a). This is caused by the damage and pinhole formation in the chemically grown SiO_x layer at this high temperature and by the excessive dopant diffusion into the c-Si.^[43–46]

The annealed samples were hydrogenated using a hydrogen-rich ALD Al₂O₃ layer to improve the surface passivation quality even further. Figure 2b shows a very large amount of hydrogen at the poly-Si/SiO_x interface in the as-deposited condition that effuses out during annealing, causing a reduction in the chemical passivation quality. During annealing after Al₂O₃ deposition, hydrogen from the Al₂O₃ layer diffuses to the poly-Si/SiO₂ interface. Van de Loo et al. demonstrated in their work^[47] that the hydrogen concentration increased significantly at the poly-Si/SiO_x interface due to the hydrogen diffusion from the H-rich Al₂O_x layer. The supplied hydrogen improves the surface passivation quality by passivating defects and dangling bonds at the c-Si absorber surface.^[47]

Figure 5a illustrates the improvement of iV_{OC} of the poly-Si contact on planar wafers from 701 to 712 mV after hydrogenation. The J_0 of 3 fA cm⁻² has been achieved for the corresponding batch after hydrogenation, which indicates an excellent surface passivation quality of the contact. For the poly-Si contact on the textured samples, J_0 as low as 17 fA cm⁻² and iV_{OC} of 706 mV have been achieved after hydrogenation.

2.3. Junction Resistivity

Figure 4d presents the junction resistivity of the poly-Si contact annealed in different conditions. Junction resistivity values less than 15 mΩ · cm² have been realized for the poly-Si samples annealed at 900 °C, but this annealing condition causes degradation in surface passivation quality. In contrast, for the optimized annealing condition (850 °C for 30 min), junction resistivity value of around 50 mΩ · cm² has been achieved, which is still low enough for full area contacts.

Figure 4d illustrates that J_0 and junction resistivity of the APCVD poly-Si contacts are related through an exponential decay, wherein lower junction resistivity means higher J_0 . Junction resistivity depends on the sheet resistance of the doped poly-Si layer, the carrier transport mechanism (via tunneling and/or pinholes in the SiO_x layer), and the dopant diffusion into the c-Si. Higher dopant diffusion into the c-Si and damage/pinhole formation in the SiO_x layer facilitates carrier transport through the contact and thus, yields lower junction resistivity.^[43] In contrast, excessive dopant diffusion into the c-Si and any damage or pinhole formation in the SiO_x layer lowers the J_0 . Because of these reasons J_0 has an inversely proportional relation to the junction resistivity. For in situ P-doped APCVD poly-Si, though increasing dopant concentration improves the surface passivation quality, but too much dopant results in very high junction resistivity by decreasing the grain size and the carrier mobility which lowers the carrier selectivity of the contact. These factors should be considered during selecting a carrier selective contact. In Figure 4d, we can see the poly-Si batches with J_0 of around 20 fA cm⁻² (before hydrogenation) and junction resistivity of around 50 mΩ cm² that can be

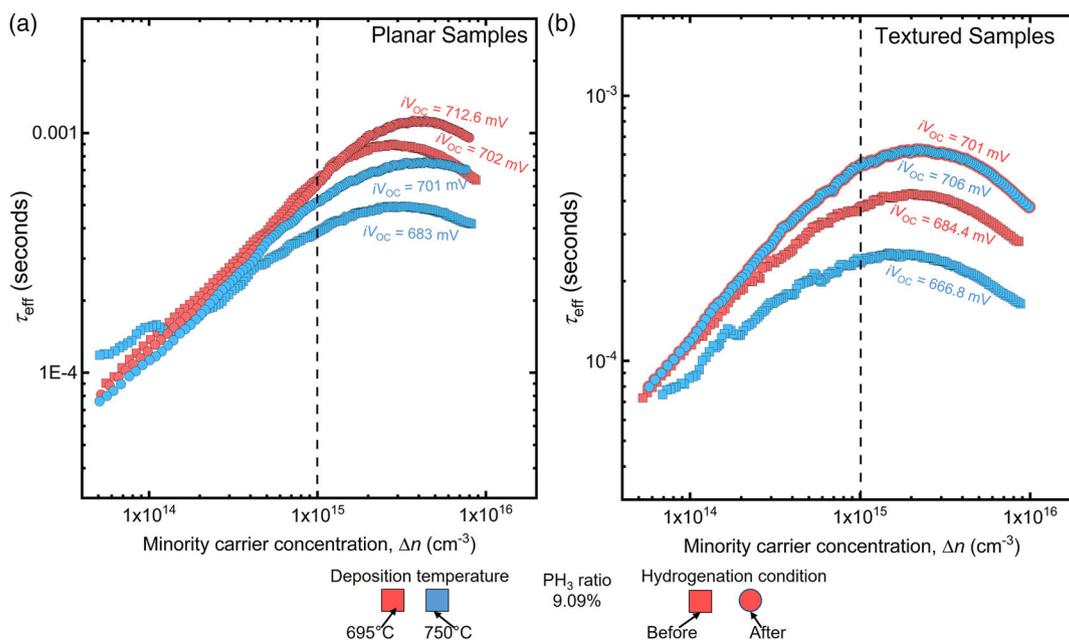


Figure 5. The injection-dependent effective minority carrier lifetime (τ_{eff}) versus minority carrier concentration (Δn) curve of 850 °C for 30 min annealed: a) planar poly-Si samples and b) textured poly-Si samples before and after hydrogenation.

considered as the optimized APCVD doped poly-Si contacts. The J_0 of these batches can be reduced further with hydrogenation which will make the contact more efficient.

3. Conclusion

In this work, passivating, electron selective contacts are fabricated using in situ P-doped poly-Si films deposited by APCVD onto a thin SiO_x layer grown by DI- O_3 . The process–structure–properties relationships of the APCVD poly-Si films are investigated in great detail. The deposition temperature, PH_3 gas ratio, and annealing temperature all impact the composition, microstructure, and electrical properties of the films, as well as the actual carrier selectivity of the contacts in terms of recombination and resistive losses.

At both deposition temperatures, the P concentration scales linearly with the PH_3 gas ratio. At a deposition temperature of 695 °C, the poly-Si films are amorphous with some evidence of nanocrystals, but at 750 °C the films are completely polycrystalline. After high-temperature annealing at all of the temperatures evaluated (820–910 °C), all of the resulting films are polycrystalline, but the crystallite size is strongly dependent on both the initial deposition temperature and the P concentration. Low deposition temperatures yield much larger crystallites, but higher P concentrations lead to smaller crystallites. These variations in the microstructure impact the conductivity of the annealed films dramatically. Although it is counterintuitive, the annealed films with higher P concentration have a higher sheet resistance. This is because the film conductivity is influenced by the average crystallite size much more than the P concentration, particularly since all of these films are heavily doped.

In terms of the performance of these passivating contacts, the post-deposition annealing temperature has a significant impact on the passivation quality and junction resistivity. As reported previously on LPCVD and PECVD films, higher annealing temperatures (i.e., 900 °C) tend to yield a less lower resistivity values, but higher recombination. Conversely, lower annealing temperatures (i.e., 850 °C) lead to less recombination, but more resistive loss. In virtually all cases, higher P concentrations in the film lead to better passivation, and the samples annealed at 850 °C performed best. Passivating contacts with J_0 values as low as 3 fA cm^{-2} have been fabricated using the 850 °C annealing temperature and a post-annealing hydrogenation process using a hydrogen-rich ALD Al_2O_3 film. Junction resistivity values of the poly-Si samples annealed at 850 °C for 30 min range from 50 to 260 $\text{m}\Omega \text{ cm}^2$, which are sufficiently low to be applied as a full area contact in c-Si PV cells.

4. Experimental Section

Symmetrical lifetime samples were prepared using 156 mm \times 156 mm pseudo-square Czochralski (Cz) *n*-type c-Si wafers with a base resistivity of 1–3 $\Omega \text{ cm}$ and thickness of 200 μm . The wafers were saw damage etched and cleaned using the standard Radio Corporation of America (RCA) process. After that, the wafers were coated with a very thin (1.5 nm) SiO_x layer grown using DI- O_3 water. An in situ P-doped Si layer was deposited on both sides of the wafers using an in-line APCVD system manufactured by Schmid Thermal Systems, Inc. In this APCVD process, silane (SiH_4) and phosphine (PH_3) gases were thermally dissociated to deposit the P-doped Si layer. The deposition process has been explained in detail previously.^[24] Different PH_3 gas ratios and deposition temperatures (T_d) (Table 1) were used to deposit the doped Si layer to observe their effect on the microstructure, electrical properties, and passivation quality of the contacts. Batches A, B, and C in Table 1 were deposited in the same deposition zone temperature of 695 °C using different PH_3 ratios of 1.48%,

4.00%, and 9.09%, respectively. For batches D, E, and F (Table 1), the PH₃ gas ratios were increased in the same order (1.48%, 4.00%, and 9.09%, respectively), but a higher deposition zone temperature of 750 °C was used. The deposition zone temperatures 695 and 750 °C yielded substrate temperatures of around 635 and 680 °C, respectively. The thickness of all of the as-deposited Si layers was around 120 nm and measured by spectroscopic ellipsometry.

The as-deposited samples were annealed in a muffle furnace in an air environment at 820, 850, 900, and 910 °C for passivation activation, solid-phase crystallization, dopant activation, and dopant diffusion into the c-Si substrate. The temperature was increased from room temperature to the targeted annealing temperature at 10 °C min⁻¹. The samples were also cooled down using a 10 °C min⁻¹ cooling rate. All the annealed samples were dipped in hydrofluoric acid (HF) before the characterization steps and the post-deposition treatments to remove the thermal oxide layer formed during the high-temperature annealing process.

Batches deposited at 695 and 750 °C with a 9.09% PH₃ ratio on both planar and textured c-Si wafers were hydrogenated using a hydrogen-rich atomic layer deposited (ALD) aluminum oxide (Al₂O₃) layer to enhance the passivation quality. For textured symmetrical sample preparation, the same wafer type and DI-O₃ oxide growth process were used. After APCVD deposition, the textured samples were annealed at 850 °C for 30 min in an air environment before hydrogenation. For hydrogenation, an ALD Al₂O₃ film of 6 nm was deposited on the annealed poly-Si samples followed by annealing at 450 °C for 20 min in an air environment to supply the hydrogen at the poly-Si/SiO_x/c-Si interface. The details of the ALD Al₂O₃ deposition process have been described in the work by Gregory et al.^[5]

The crystallinity of the as-deposited and annealed APCVD Si layers was determined by grazing incidence X-ray diffraction (GI-XRD) and Raman spectroscopy. GI-XRD measurements were performed using a PANanalytical Empyrean System. The XRD spectra were obtained using Cu-Kα radiation with a wavelength of 1.54 Å at a fixed incidence angle of $\omega = 5^\circ$. The incidence angle was kept low enough so that all the data was collected only from the APCVD Si films.

Raman spectroscopy was performed on a Horiba® LabRam HR Evolution system with a 473 nm excitation wavelength. This blue laser allows for a short penetration depth. A 100× objective, 1800 gratings mm⁻¹, and 10% neutral density filter were used for the single point scans. A laser intensity of 1.9 mW with a spot diameter of 641 nm was used for the scans. The experimental conditions were 5 s integration time and 5 accumulations. Prior to conducting any Raman measurements, the equipment was calibrated using a standard calibration objective.

The surface topography of the APCVD Si layers was characterized using AFM. To prepare the samples for AFM measurements, APCVD Si films were deposited on a mirror polished Si wafer. AFM scans were performed in tapping mode using the Veeco/DI Dimension 3100 AFM system over 1 μm² surface area.

As the passivation quality and carrier selectivity of the doped poly-Si contacts largely depend on the P and hydrogen concentration in the films and at/near interfaces, dynamic secondary ion mass spectroscopy (SIMS) measurement was performed on the samples to acquire P and hydrogen depth profiles. A PHI Adept 1010 Dynamic SIMS system was used to perform the measurement using cesium (Cs) ion beam with 3 kV energy as the primary beam with 300 μm raster size, 5% detection area, and 40–50 nA beam current. The sheet resistance of the doped poly-Si layers was measured using an Ossila four-point probe system. Symmetrical lifetime samples were used to perform this measurement.

The passivation quality of the samples was investigated by measuring the saturation current density (J_0) and implied open-circuit voltage (V_{OC}) using photoconductance measurements with a Sinton Instruments WCT-120.^[48] J_0 values were extracted from the Auger corrected inverse effective minority carrier lifetime versus minority carrier concentration plots using the Kane–Swanson method.^[49] Photoluminescence (PL) imaging was also performed on the samples to evaluate the passivation quality. PL images were taken using a BT Imaging LIS-R1 system under 1 sun conditions, assumed to be a photon flux of $3.085 \times 10^{17} \text{ cm}^{-2} \text{ s}^{-1}$. This system features a laser of 808 nm as the optical excitation source, a 920 nm

long-pass filter to remove the reflected light, and a 1-megapixel Si charge-coupled device (CCD) camera to capture the emitted PL response.^[50]

Contact and junction resistivities of the poly-Si contact were measured using the transmission line method (TLM)^[51] using a BrightSpot ContactSpot tool.^[52–54] For the metal contact formation on the poly-Si layer, TLM pads with 5 mm length and 2.5 mm width were deposited using an e-beam evaporated 30 nm titanium (Ti) layer capped by around 300 nm aluminum (Al) layer. TLM pads were deposited with varying gaps in between them. The poly-Si film in between the TLM pads was completely etched with reactive ion etching (RIE) process using sulfur hexafluoride (SF₆) gas to force current through the poly-Si and SiO_x layers and into the c-Si absorber.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the Solar Energy Technologies Office Agreement Number DE-EE0008980. This work was also partially supported by the UCF Office of Research through an Interdisciplinary Research award. Use of HORIBA LabRam confocal Raman is possible with support from NSF MRI Award Number 1920050. The Materials Characterization Facility (MCF) at the University of Central Florida (UCF) is acknowledged for the usage of its facilities.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

APCVD, microstructure, passivating carrier selective contacts, POLO, polycrystalline silicon, solar cells, TOPCON

Received: December 14, 2021

Revised: January 21, 2022

Published online:

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