High voltage fast ramp pulse generation using avalanche transistor

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The authors have developed an avalanche transistor based pulser for use as a pockel cells driver and for gating a microchannel plate. The output voltage ranges from 1–4 kV to 50 Ω, with fall times of 200–300 ps. The repetition rate is less than 1 kHz. The trig jitter is less than 100 ps. Trig delay is about 8 ns. © *1998 American Institute of Physics.* [S0034-6748(98)02607-0]

I. INTRODUCTION

High voltage ultrafast electrical pulse has been widely used in laser technology, high speed photography, and nuclear physics. Some typical applications are sweeping circuits for streak camera, gating microchannel plate, driving the pockel cells, and laser diode. In this article, we present a design for high speed, high voltage ramp pulse generator using avalanche transistors. This circuit consists of five strings of avalanche transistors which are connected in the Marx bank configuration.[1–4] As with any very high speed circuit, layout is important. Note 50 Ω transmission line structure is designed to minimize stray inductance and decrease the rise time of output pulse.

II. THEORY OF OPERATION

The working theory of the avalanche transistor is well known. For single avalanche transistor the output current is expressed by

$$I_L=(V_{\mathrm{CBO}}-V_{\mathrm{CEO}})/R_L, \tag{1}$$

where R_L is load resistor. V_{CBO} is the breakdown voltage when base and emitter are connected, V_{CEO} is the breakdown voltage when base and emitter are open.

The conventional approach to increase the output voltage is to use a string of avalanche transistors, or a Marx bank-type design. The Marx bank-type design has the advantage of a lower power supply voltage, but at the cost of much more stored charge. The advantage of a single long string of avalanche transistors is that it reduces the total stored charge of the system, which prevents damage to the pulser due to self-trigger or breakdown. The disadvantage with this circuit is that the DC power supply voltage cannot be very high, otherwise it will produce a corona. The combination of the two types of design is an ideal method to produce high voltage ultrafast pulses. Figure 1 is the schematic diagram of our circuit.

This circuit consists of five strings of avalanche transistors which are mounted on a 50 Ω transmission line. There are eight transistors in each string. In order to keep stray inductance to minimum, the capacitors are formed by pads on the double-sided printed circuit board. The inductance of the transistors and the PC board capacitors form a 50 Ω coplanar waveguide transmission line structure. The first transistor (Q_{11}) in the first string is triggered via a small ferrite bead pulse transformer (T_1). When Q_{11} is triggered, this places the collector of the first transistor (Q_{11}) near ground potential, resulting in about 700 V collector-to-emitter voltage across the second transistor (Q_{12}). The second transistor suffers a nondestructive avalanche breakdown due to this overvoltage. As each transistor turns on, the next suffers an even greater overvoltage resulting in faster rise time and shorter delay. At last the final transistor (Q_{58}) turns on and a high voltage, fast rise time pulse is produced.

The positive and negative power supplies (± 1.5 kV) are connected to each string of transistors through double 2 MΩ resistors. The standby current in each string is limited to less than 50 μA. This small bias current is helpful to improve the stability of this circuit. The output pulse width is limited to less than 15 ns, because we have found that these transistors tend to burn out in a short time if the pulse width is wider. There are two advantages of this configuration.

(1) Relative lower voltage power supply is used. This prevents producing a corona in this circuit.
(2) It is helpful to shorten the rise time of the output pulse.

III. COMPONENT SELECTION

The avalanche transistors used are 2N5551, the V_{CBO} of transistor is about 350 V, V_{CEO} is about 200 V. We have

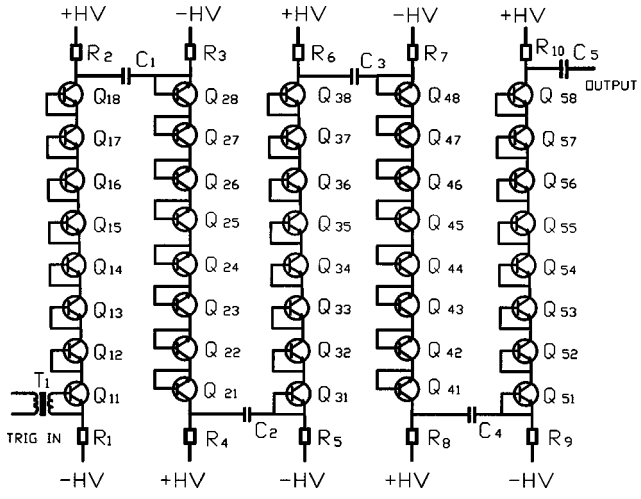

FIG. 1. High voltage pulse generator circuit.

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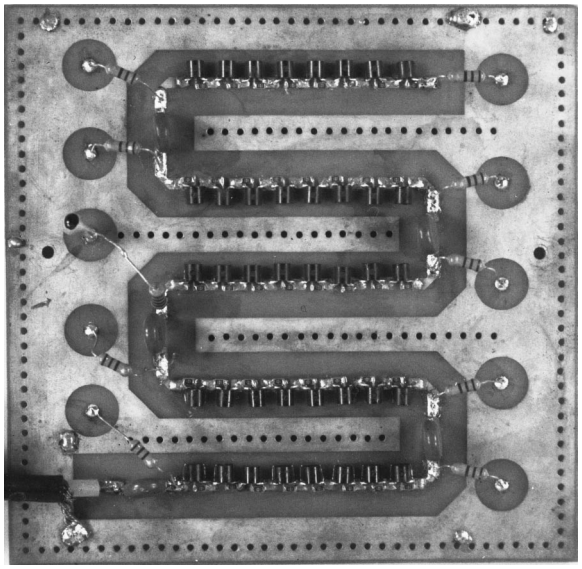

FIG. 2. Photograph of the high voltage circuit.

noted that the difference of breakdown voltage of this kind of transistor is much greater, and the breakdown voltage drifted during the test. This will result in a change of trigger delay and output swiching voltage. In order to resolve these problems, an avalanche transistors ''burn-in'' tester was used to ''cook'' a number of transistors for several months. We

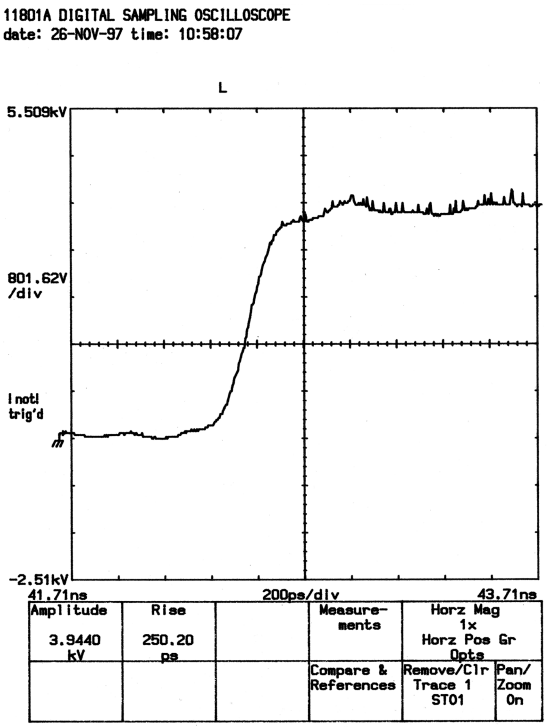

FIG. 3. Ramp pulse with rise time 250 ps, amplitude 4 kV.

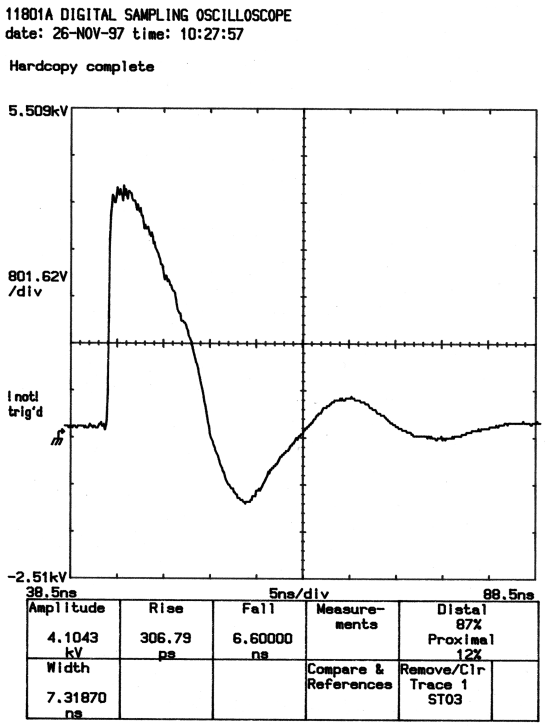

FIG. 4. Entire output pulse wave form from this circuit.

selected the transistors with the same breakdown voltage, the same trigger delay, the same rise time, and with small trigger jitter.

IV. CIRCUIT DESIGN AND MEASUREMENT RESULT

The rise time of output pulse is basically determined by the stray capacitance in the last string and by how fast the last string of transistors turns on. Determination of the stray capacitance in the last string is fairly simple. Figure 2 is the photograph of this circuit.

The circuit should have a 50 Ω impedance to match the load. Assuming the inductance of each avalanche transistor is 2 nH, the total inductance in the last string (eight transistors) is 16 nH. The stray capacitance in the last string can be calculated by

$$Z=\sqrt{\frac{L}{C}}\Rightarrow C=\frac{L}{Z^2}\Rightarrow C=\frac{16\ \text{nH}}{50^2}=6.4\ \text{pf}. \tag{2}$$

Using this data we can calculate the rise time of output pulse, $RC=50\ \Omega\times 6.4\ \text{pf}=320\ \text{ps}$. The stray capacitance is formed by the pads on the printed circuit board. Figure 3 is the output ramp pulse from this circuit measured by the oscilloscope Tek 11801A and attenuators which are manufactured by Barth electronics, Inc. Figure 4 is the entire pulse.

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