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High-contrast, all-silicon waveguiding platform for ultra-broadband mid-infrared photonics

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Suspended silicon-membrane ridge waveguides are fabricated and characterized on a single-material photonic device platform. By using direct bonding, a thin layer of silicon is fused to a bulk silicon substrate, which is patterned with narrow trenches. Waveguides are etched on the resulting suspended membranes and are characterized at mid- and near-infrared wavelengths. Transverse magnetic-mode propagation losses of 2.8 ± 0.5 and 5.6 ± 0.3 dB/cm at 3.39 and 1.53 μm wavelengths are measured, respectively. This all-silicon optical platform is capable of continuous low-loss waveguiding from wavelengths of 1.2–8.5 μm, enabling numerous applications in frequency conversion and spectral analysis. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4824771]

Silicon photonics is a mature field for optical devices for near-infrared (IR) wavelengths.[1] Intrinsically, silicon exhibits low material-induced optical loss up to a wavelength of 8.5 μm,[2] making it a potentially useful material for waveguiding at mid-infrared (mid-IR) wavelengths.[3] If mid-IR silicon photonics can be combined with the complementary metal–oxide–semiconductor (CMOS) technology of microelectronics, devices for a host of applications can be realized at low cost and high volume.[2] However, many challenges still exist for improving the compatibility of silicon photonics with the CMOS process.[4]

The platform of choice for near-IR silicon photonics is currently silicon-on-insulator (SOI), but the bottom cladding layer of silicon dioxide causes large optical loss across most of the mid-IR range,[5] although certain devices can be made to operate in limited transparency windows.[6] Alternative platforms have been proposed and explored, which avoid this problem. Silicon-on-sapphire (SOS) is an existing wafer technology that has recently been used to obtain mid-IR waveguides with losses as low as 0.7 dB/cm,[7,8] but the transparency window is limited by the onset of sapphire absorption starting at 4.4 μm. We have recently demonstrated silicon-on-nitride (SON) waveguides with moderate losses of 5.1 dB/cm, transparent up to 6.7 μm.[9]

To obtain the mentioned largest intrinsic transparency window of silicon, the influence of cladding materials can be removed altogether. Suspended membrane waveguides benefit from this, and mid-IR optical losses of 3 dB/cm have been demonstrated from membranes on SOI wafers.[10] The lossy buried oxide (BOX) layer is locally removed under ridge waveguides through a series of holes adjacent to the waveguide. However, this approach requires that the etched holes be sufficiently far from the waveguide so as to not perturb the optical mode. This results in very wide membranes with poor support and high flexure, since the oxide is removed equally in both directions from the holes. The problem is compounded for longer wavelengths, when the etched-hole separation increases. Furthermore, the trench depth must be increased to avoid radiation loss into the substrate when longer wavelengths are considered. Finally, since the BOX layer must have the same thickness as the trench, it forms an increasingly thick thermal barrier, constraining heat dissipation performance. With an ultimate goal of CMOS compatibility and practical production, these challenges must be considered in the design of a mid-IR photonic platform.

In this work, we have built on the previous suspended-membrane waveguide research and designed a new platform that addresses many of the above practical issues facing photonic device fabrication. Using direct silicon bonding, a thin silicon membrane is fused to a bulk silicon substrate that has been pre-patterned with trenches, forming highly compact suspended membranes on this all-silicon optical platform (ASOP). Waveguides are then formed by standard lithographic techniques on the membranes (Fig. 1). The detailed fabrication process is described later in this Letter. The ASOP frees us from many constraints inherent to SOI-based membranes. Since the trenches are formed on a separate substrate, any depth can be chosen to suit the wavelength and substrate leakage requirements. Additionally, since there are no etched holes or perforations, the membrane is much stronger and exhibits less flexure. As a result, the waveguides can be etched deeper, and the membrane width can be shrunk to unprecedented values. The combination of arbitrary trench (lower cladding) depths and greatly reduced minimum membrane widths allows the ASOP to guide light over silicon's transparency range of 1.2 to 8.5 μm; the loss figure is unaffected by any external material limitations. Combined with silicon's intrinsically high third-order nonlinear optical properties, the ASOP will enable nonlinear optical functions over an unprecedented bandwidth through effects such as Raman lasing and amplification,[11,12] four-wave mixing,[13] and third-harmonic generation.[14] To further demonstrate the robustness of ASOP waveguides, COMSOL^{TM} simulations were conducted to confirm that low-loss mid-IR waveguiding at the wavelength of $\lambda = 3.39$ μm with a total membrane width of only 5 μm is feasible. The leakage loss into the bulk silicon accounts for <0.1 dB/cm for both the transverse electric (TE) and transverse magnetic (TM) polarizations. Such a

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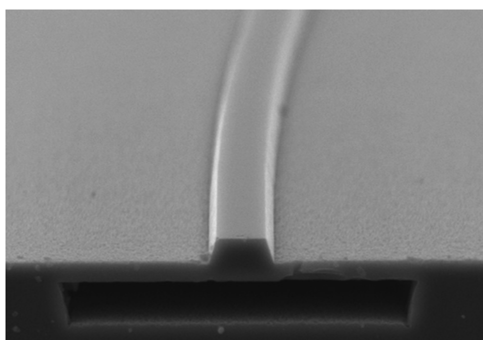

FIG. 1. Scanning electron microscope (SEM) image of a fabricated waveguide. The fabricated waveguides are 2.4 μm wide and have ridges that extend by 1.07 μm above the membrane. The membrane width is 17 μm, and the trench depth is 2 μm. No boundary is visible between the bonded silicon layer and the bulk substrate, indicating the high quality of the achieved fusion bond.

design is not practical with the previously reported SOI-based membrane waveguides.

Our approach offers other advantages, including enhanced device-layer thermal conductivity[15] and the option for low-resistance contacts to the substrate to be formed at the bonding interface when hydrophobic bonding techniques are used.[16] In this way, a photonic device can be fully patterned and delivered to a CMOS foundry that processes bulk silicon, rather than SOI, substrates. All of these advantages represent a significant step forward in the realization of a practical mid-IR photonic device platform.

A schematic of the fabrication process is provided in Fig. 2. The first step in fabrication is the preparation of the handling die onto which a thin silicon layer will later be bonded. Optical lithography and inductively coupled plasma reactive ion etching (ICP RIE) were used to fabricate 2 μm-deep trenches on bulk silicon substrates. Next, a small SOI die about $1 \times 1\,\text{cm}^2$ with a top silicon thickness of $\sim$2.14 μm was prepared. Both the SOI die and the handling die were simultaneously subjected to oxygen plasma treatment, which rendered them hydrophilic. They were each dipped in deionized water for 15 s and blow-dried using a nitrogen gun for 15 s. Then, the SOI die was carefully inverted and placed on top of the handling die, such that the top silicon layer came in contact with the trench-patterned surface. The dies were then placed inside a steel clamp and held under moderate pressure at 300 °C for 30 min to initiate low-temperature bonding.[17] The bonded sample was then removed, and a high-temperature oxidation step was performed at 950 °C in a wet oxygen environment, forming approximately 40 nm of silicon dioxide on the backside of the handling die, and on the inner sides of the trenches. This thin oxide layer protected the membranes from tetramethylammonium hydroxide (TMAH) wet etching later. The SOI wafer backside was selectively removed using a two-step wet etching process with HNA (hydrofluoric acid, nitric acid, and acetic acid) and TMAH etching. After the backside wet-etching was completed, waveguides were fabricated over the now-exposed suspended membranes using standard optical lithography. The waveguides were found to be 2.4 μm wide, with 1.07 μm thick membranes (slabs) and 1.07 μm thick ridges. The sample was then cleaved, diced, and polished on two edges to form smooth waveguide facets. The fact that the membranes endured the intense stresses of polishing, cleaving, and dicing is a testament to their strength.

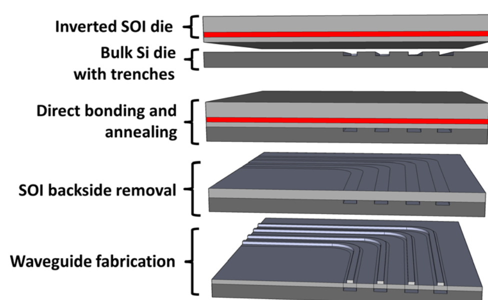

FIG. 2. Simplified representation of the fabrication process used to produce ASOP waveguides.

Overall, the bond quality is very high, with only a few unbonded regions in the various samples. In some cases, small bubbles appeared, but occupied only a very small fraction of the chip. The average yield for most samples was over 90% at the point of backside removal. A few waveguides were damaged during the dry etching procedure, most likely due to the $\pm$25% non-uniformity of the silicon device layer thickness from the SOI substrate. It is also important to consider that this particular fabrication approach is chosen only because of the limited available equipment. When extended to a commercial process, a combination of ion-implantation, chemical mechanical polishing (CMP), and machine-automated wafer bonding may be used. This is a well-known process used to economically produce many technologies, including SOI wafers.[18]

The ASOP-based waveguides were then characterized to determine their optical propagation loss. The exact reflectivity of the waveguide facets, necessary for Fabry-Perot loss measurements, was determined by a full 3D finite-difference time-domain (FDTD) simulation using the free, open-source MEEP software package.[19] Our custom simulation approach is depicted in Fig. 3. The fundamental mode is excited at the beginning of the waveguide and traverses a power monitor boundary, which registers the input power level. When the optical wave reaches the boundary, some of its energy is reflected off the perpendicular air interface, and some is transmitted and absorbed by the boundaries. The reflected portion in the waveguide passes through the power monitor

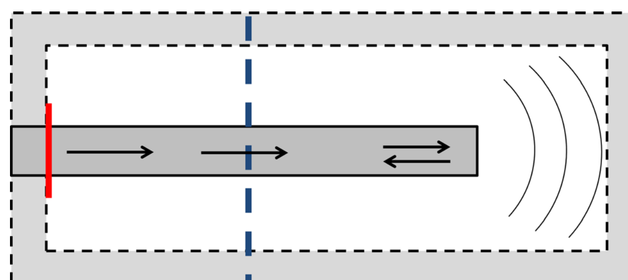

FIG. 3. Schematic view of the 3D simulation used to determine the precise reflection coefficient of the fabricated waveguide facets. The red boundary is the source excitation point, the blue dashed line is the power monitor location, and the gray shaded region is the perfectly absorbing boundary space. Power flow is indicated at a particular point in time as forward or backward arrows and radiating arcs.

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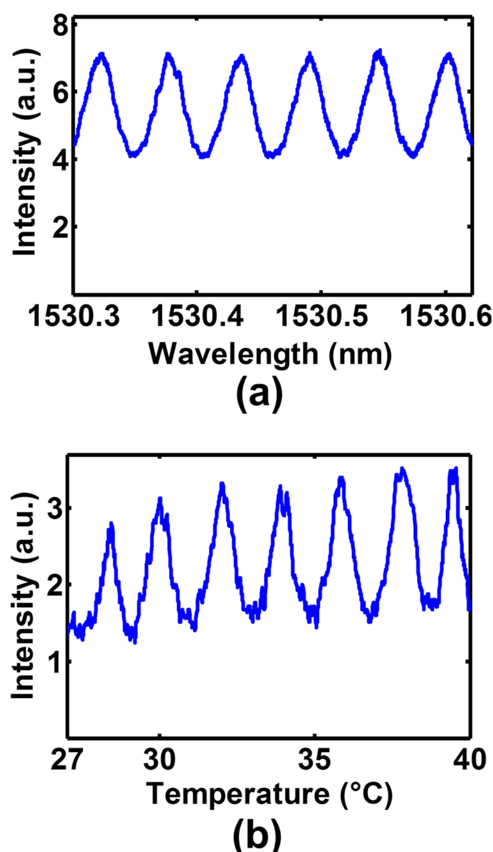

FIG. 4. Fabry-Perot interference fringes recorded from a fabricated waveguide; (a) TE-mode near-IR data obtained by sweeping a tunable source at $\lambda = 1.53\,\mu$m; (b) TE-mode mid-IR data obtained by tuning the temperature of the chip from 27 to 40 °C.

again, causing a change in the power flow vector which indicates the amount reflected. The simulation was tested to confirm that boundary reflections and scattered light had only a small effect on the result. This was achieved by monitoring the optical power at several locations along the waveguide and averaging the calculated values. The simulated single-facet reflectivity $R = 0.35$ for the mid-IR TE-polarized mode is significantly different from that predicted by the generic Fresnel equation (which predicted $R = 0.29$). This discrepancy is a known characteristic of optical guided modes with highly diverging output beams.[20]

Near-IR propagation loss measurements were conducted in order to obtain accurate lengths of the waveguides and to assess the short-wavelength performance. An optimal TE-mode loss of 5.4 ± 0.2 dB/cm and a TM-mode loss of 5.6 ± 0.3 dB/cm were obtained by scanning a semiconductor tunable laser source from 1530 to 1531 nm (Fig. 4(a)).

Next, the waveguides were characterized using a 2 mW Helium-Neon (HeNe) laser at 3.39 μm to determine their mid-IR performance. The photonic chip was placed on top of a thermo-electric cooled pad, which enabled the measurement of Fabry-Perot interference fringes through temperature tuning. The experimental measurement method and setup is the same as in our previous work on SON waveguides.[9] The lowest loss observed for the TE-polarized mode was 4.0 ± 1 dB/cm. The TM-polarized mode exhibited a minimum loss of 2.8 ± 0.5 dB/cm. The waveguides had a length of about 5–7 mm. Examples of the recorded data are presented in Fig. 4(b). The propagation loss is probably due to small defects in the waveguides from lithography and from roughness of etched sidewalls.

The waveguides exhibited somewhat higher propagation loss at near-IR wavelengths compared to mid-IR. A similar discrepancy was observed in our previous work on SON waveguides.[9] A probable explanation for this is a partial coupling of input light into higher-order modes when measuring at near-IR. Since these modes (which are confirmed to exist in simulations) have greatly increased propagation loss compared to the fundamental mode, the fringe contrast in Fabry-Perot measurements is reduced, leading to a higher apparent propagation loss value.

In summary, a single-material waveguiding platform for future mid-IR photonic applications, the ASOP, is demonstrated. By using direct bonding, totally unperforated, air-clad silicon membranes were fabricated and patterned with low-loss waveguides. The fabricated waveguides have a minimum mid-IR TM-mode propagation loss of 2.8 dB/cm, and a width footprint of only 17 μm, which can easily be reduced to 5 μm or less. The ASOP represents a significant improvement on the previous suspended-membrane waveguide technology, with greater mechanical robustness, a more compact waveguide footprint, and better scaling to longer wavelengths due to the elimination of geometrical trade-offs with trenches and etch-holes. Furthermore, it has better CMOS compatibility than other currently demonstrated mid-IR photonic platforms, opening the way to advanced photonic integrated systems for sensing and analysis applications.

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