Pixel Circuit with Bootstrapping Structure for Blue-Phase Liquid Crystal Display

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Abstract

This work presents a new pixel circuit designed on glass by using hydrogenated amorphous silicon (a-Si:H) technology for polymer-stabilized blue-phase liquid crystal (BPLC) display with vertical field switching (VFS) mode. In the VFS mode, the driving voltage of BP-LC can be reduced, moreover, the hysteresis and residual birefringence are effectively suppressed as well. From the simulation results, the average error rate of storage voltage in pixel circuit is below 5.14% while operating frequency is 180 Hz.

1. Introduction

Polymer-stabilized blue-phase liquid crystal (PS-BPLC) displays have attracted considerable attention and been expected to become the next generation displays due to their fast gray-to-gray response time, no need for alignment layer, submillisecond response time, and isotropic dark state [1]-[3]. Especially, the fast response time can help enable color sequential display, so that the light efficiency and resolution density can be tripled. Recently, in-plane switching (IPS) electrodes are widely used in PS-BPLC displays because the backlight can be set at normal incidence, also, high contrast and wide view can be achieved easily [4]. However, high driving voltage (>50 V) and large hysteresis caused by the strong electric fields at the edge of electrodes are critical issues [5], [6]. Although some methods, such as protrusion electrodes [5], wall-shaped electrodes [7], double-penetrating fringe fields [8], and corrugated electrodes [9], have been published to improve the high driving voltage and hysteresis, the complicated manufacturing process should be considered. To solve the complicated fabrication problem, vertical field switching (VFS) mode with simple cell structure and uniform electric field has been proposed. It helps reduce the driving voltage and suppress hysteresis [10]. The major challenge for the VFS mode is to achieve wide viewing angle and high contrast ratio. For both IPS and VFS mode, a high Kerr constant is required in order to reduce the driving voltage. The major approach to achieve a high Kerr constant is to employ a LC with large dielectric anisotropy, which produces a large capacitance (Clc) of BPLC, leading to insufficient charging capability in conventional pixel circuit, i.e. the voltage applied on LC cannot reach the desired value within the charging time. Especially, in color sequential displays, the driving frequency is tripled, so that the charging problem will be more severe.

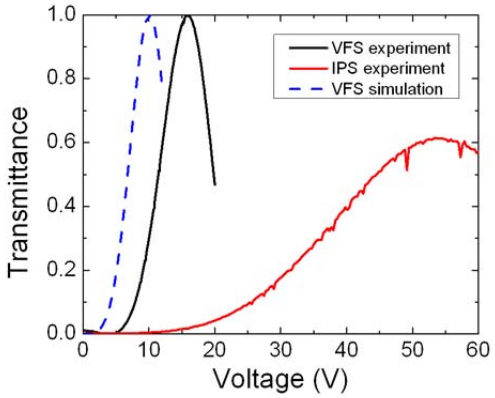

Fig. 1. Measured VT curves for VFS (black) and IPS (red) cells at room temperature (T ~23°C). Incident angle θ = 70° and λ = 633nm. Dashed blue line is simulated curve for a VFS cell with cell gap 3μm, incident angle 75° and λ = 550nm.

In the paper, we investigated the driving capability of pixel circuit for large capacitances and proposed a new driving circuit. Compared to conventional pixel circuit, the newly proposed pixel driving circuit employs an additional signal to keep the aperture ratio and improve the insufficient charging capability of pixel circuit.

2. Proposed Pixel Circuit

Fig. 1 shows voltage-dependent transmittance (VT) curves for IPS and VFS cells. The electrode width/gap/cell gap for the IPS cell is 10/10/7.5 μm. The cell gap for the VFS cell is 5.7μm. The material preparation process is described as follows: The BPLC material employed is Chisso JC-BP01M [10]. The material is injected to both IPS and VFS cells by capillary filling. The phase transition temperature is BP 42.4°C N* during the cooling process and N* 44.5°C BP during the heating process, where N* stands for chiral nematic phase and BP stands for blue phase. UV irradiation process was performed at 44°C with an intensity of 2 mW/cm^2 for 30 min. After UV curing, the

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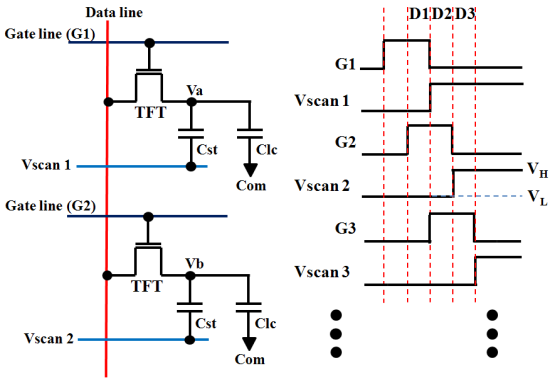

Fig. 2. Proposed driving scheme and its timing diagram.

VT curves are measured at room temperature using He-Ne laser (633nm). The measurement method can be found in Ref. 10. The incidence angle is set at 70°. From Fig. 1, the VFS cell (black line) has much lower voltage than IPS cells (red line). To further reduce the driving voltage to ~10V, we reduced the cell gap to 3μm, increased the incident angle to 75° and changed the central wavelength to 550 nm. The dashed line shows simulated curve and its capacitance is easy to be calculated by the following equation:

$$Clc = \frac{\varepsilon \times \varepsilon_0}{d} \times A \qquad (1)$$

where the ε, d, and A are the relative dielectric constant, the thickness of the BPLC cell (cell gap), and the total area of the BPLC cell, respectively. The ε_0 is 8.854×10^{-12} F/m. In this case, ε is 72 at room temperature and voltage off state. For a pixel size of 120 μm× 360 μm, the calculated LC capacitance is ~9 pF, which is much larger than the traditional nematic LC. Therefore, although VFS cell has lower driving voltage and smaller hysteresis, a suitable driving scheme which can improve the charging capability is the major study in the following discussion.

Fig.2 shows the newly proposed driving scheme and its timing diagram for BP-LCDs. A thin-film transistor (TFT) is controlled by the gate line while the data line provides a data voltage for the pixel circuit. Cst in the pixel circuit is a storage capacitor used to memorize the data voltages. Clc is the effective capacitor of BPLC. Moreover, an additional control signal (Vscan) is used to supply two constant voltages (V_H and V_L) by the capacitor coupling of Cst.

Circuit operations can be divided into two following stages:

A) First period: when the gate line (G2) goes to high voltage and the G1 is kept at high voltage, the data voltage (D1) is transmitted to Va node of the current pixel circuit and can pre-charge Vb node of the next pixel circuit to extend the charging time. Then, G1 is changed from high to low voltage and the new data voltage (D2) is supplied to Vb node of pixel circuit.

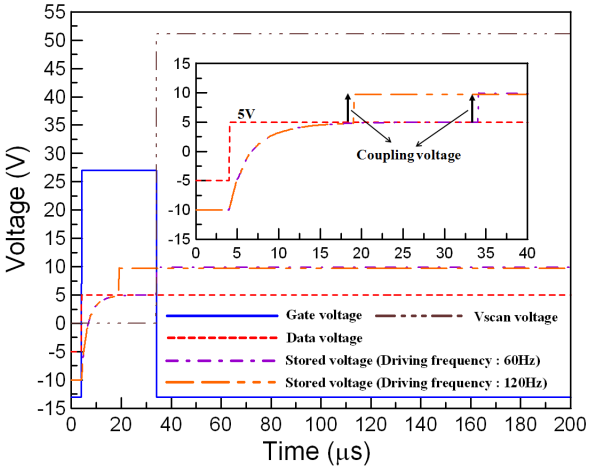

Fig. 3. Stored voltages of proposed structure in Cst with a data voltage of 10 V.

B) Second period: when the gate line (G2) goes to low voltage, the additional signal (Vscan 2) is changed from V_L to V_H to couple a constant voltage (ΔV) to the Vb node. Therefore, the stored voltage of Vb node can be expressed as follow:

$$Vb = D2 + (V_H - V_L)\frac{Cst}{Cst + Clc + Ceq} \qquad (2)$$

where the Ceq is the parasitic capacitance of TFT.

Compared to the conventional pixel circuit, the new driving scheme via capacitor coupling method can reduce the data voltage swing, enhance the driving capability, and improve power consumption of the panel.

3. Measurement Results and Discussion

The stored voltage in pixel circuits is simulated using software HSPICE. Also, the characteristics of the TFT are matched using the Rensselaer Polytechnic Institute (RPI) model (Level = 61). The width, length, Cgd, and Cgs of driving TFT are 96 μm, 5.5μm, 3 fF, and 9fF, respectively. Voltage swings of gate line and data line are -13 V to 27 V and -10 V to 10 V. Cst and cell gap are 1 pF and 3 μm, respectively. Clc is set to 9 pF for a 120 μm× 360 μm pixel size. Also, the value of Vswing is dependent on the Cst and Clc. Therefore, to obtain the 5 V coupling voltage in this case, the Vswing is designed from 0 V to 51.1 V and can be modified in varied conditions, such as low driving voltage and low capacitance of BPLC in small pixel size. In addition, while assuming that a FHD (1920×1080) display is used, the gate pulse widths of each R, G, B subpixel are 30 μs, 15 μs, and 10 μs with a pre-charge method for 60 Hz, 120 Hz, and 180 Hz refreshing frequencies, respectively.

Fig. 3 shows the data voltage is 5 V and combined with a capacitor coupling method. When the driving frequencies are 60 Hz and 120 Hz, the stored voltages of new proposed pixel circuit are 10 V and 9.84 V, respectively. The voltage error of proposed pixel circuit is improved and reduced to 1.6 %. Fig. 4 shows the

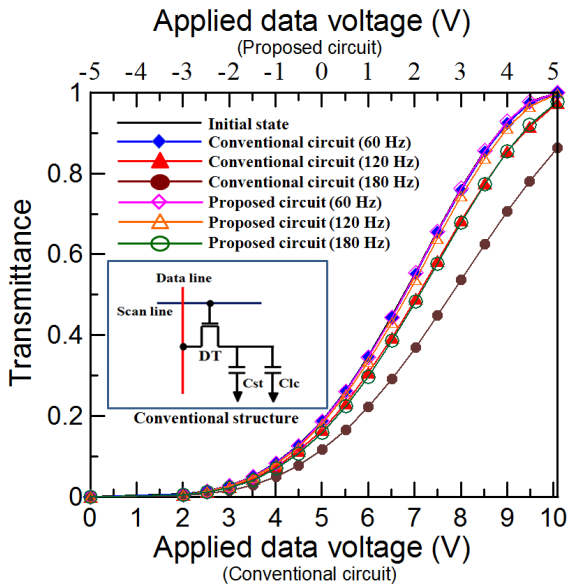

Fig. 4 Simulated VT curves of initial state, conventional circuit, and proposed circuit.

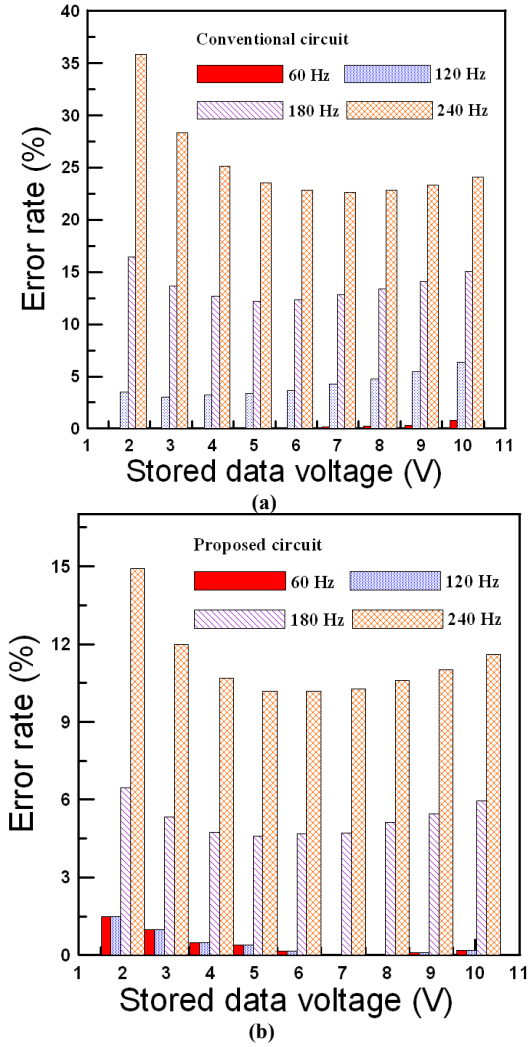

Fig. 5 Simulated stored voltage error rates at varied frequency. (a) conventional circuit (b) proposed circuit.

and proposed circuit. Compared to the initial state, the VT curves of conventional circuit and proposed circuit are matched while operating frequency is 60 Hz. However, it can be observed that the VT curves of conventional circuit reduce obviously at 120 Hz and 180 Hz operating frequency. From the simulated results, the transmittance of the conventional circuit is decayed to 0.863 and that of proposed circuit is only decreased to 0.976 when the applied voltage of conventional circuit and proposed circuit are 10.08 V and 5.08 V, respectively.

Fig. 5 indicates the stored voltage error rate of conventional circuit and proposed circuit while operating frequency is 60 Hz, 120 Hz, 180 Hz and 240 Hz. As shown in Fig. 5(a), the average error rate of conventional circuit at 180 Hz is 13.5% and that of proposed circuit at 180 Hz is 5.14%. Although the error rate achieved using the proposed pixel circuit is increased at 240 Hz, it is 55.6% smaller than that of the conventional pixel circuit. We believe this error rate can be further reduced. Therefore, based on simulation results, the proposed pixel circuit can stably store the data voltage to drive the BPLC effectively.

4. Conclusion

The new driving scheme using a-Si:H TFT for BP-LC displays with VFS mode is proposed. Compared to the conventional pixel circuit, the proposed pixel circuit offers superior performance in stored voltage while operating at high frequencies. Based on simulation results, the average stored voltage error rate at 180 Hz operation is below 5.14 % and is still acceptable for color sequential display applications.

5. Acknowledgment

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6. References

[1] H. Kikuchi, M. Yokota, Y. Hisakado, H. Yang, and T. Kajiyama,"Polymer-stabilized liquid crystal blue phases," Nat. Mater., vol. 1, pp. 64-68, 2002.

[2] Y. Haseba, H. Kikuchi, T. Nagamura, and T. Kajiyama, "Large electrooptic Kerr effect in nanostructured chiral liquid-crystal composites over a wide temperature range," Adv. Mater., vol. 17, p. 2311, 2005.

[3] J. Yan, L. Rao, M. Jiao, Y. Li, H. C. Cheng, and S. T. Wu, "Polymerstabilized optically isotropic liquid crystals for next-generation display and photonic applications," J. Mater. Chem., vol. 21, pp. 7870-7877, 2011.

[4] Z. Ge, L. Rao, S. Gauza, and S. T. Wu, "Modeling of blue phase liquid crystal displays," J. Display Technol., vol. 5, no. 7, pp. 250-256, Jul. 2009.

[5] L. Rao, Z. Ge, S. T. Wu, and S. H. Lee, "Low voltage blue-phase liquid crystal displays," Appl. Phys. Lett., vol. 95, p. 231101, 2009.
[6] M. Sato and A. Yoshizawa, "Electro-optical switching in a blue phase III exhibited by a chiral liquid crystal oligomer," Adv. Mater., vol. 19, p. 4145, 2007.
[7] M. Kim, M. S. Kim, B. G. Kang, M. K. Kim, S. Yoon, S. H. Lee, Z. Ge, L. Rao, S. Gauza, and S. T. Wu, "Wall-shaped electrodes for reducing the operation voltage of polymer-stabilized blue phase liquid crystal displays," J. Phys. D: Appl. Phys., vol. 42, p. 235502, 2009.
[8] L. Rao, H. C. Cheng, and S. T. Wu, "Low voltage blue-phase LCDs with double-penetrating fringe fields," J. Display Technol., vol. 6, no. 8, pp. 287-289, Aug. 2010.
[9] M. Jiao, Y. Li, and S. T. Wu, "Low voltage and high transmittance blue-phase liquid crystal displays with corrugated electrodes," Appl. Phys. Lett., vol. 96, p. 011102, 2010.
[10] H. C. Cheng, J. Yan, T. Ishinabe, N. Sugiura, C. Y. Liu, T. H. Huang, C. Y. Tsai, C. H. Lin, S. T. Wu, "Blue-phase liquid crystal display with vertical field switching," J. Display Technol., vol. 8, no. 2, pp. 98-103, Feb. 2012.