New Blue-Phase LCD Driving Pixel Circuit for a-IGZO TFT with Large Operation Voltage

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Abstract

A new pixel circuit for driving blue-phase liquid crystal displays is proposed. To increase the transmittance of blue-phase liquid crystals, the proposed circuit enlarges the range of the operating voltage. Simulation results show that the operating voltage can be successfully increased and the error rates are all less than 5%.

Author Keywords

Blue-phase liquid crystal; large operation voltage; pixel circuit

1. Introduction and

Blue-phase liquid crystal (BPLC) is considered as the candidate of the next-generation display technology owing to their submillisecond response time, reduction of the molecular alignment layer, and cell gap insensitivity [1]-[3]. Such characteristics reduce the motion blur while displaying the fast-moving images and enable color sequential displays employ RGB LEDs which will triple the resolution by eliminating the color filter [4], [5]. Furthermore, applying in-plane switching (IPS) electrode in BPLCD can effectively increase the contrast ratio and the viewing angle of the displays because the backlight can be set at normal incidence [6], [7]. However, BPLCs have higher operation voltage and relatively low transmittance compared with the conventional nematic LCs [5]-[7], becoming the obstacles of the widespread application of BPLC. Several researches [8]-[10] have been proposed to improve the drawbacks of the BPLCs. Rao *et al*. [8] proposed a protrusion electrode structure to lower the operation voltage of the BPLCs to ~10 V_{rms} and achieve high transmittance (~70%). Rao *et al*. [9] also proposed a new IPS structure with double-penetrating fringe fields to reduce the operation voltage and widen the viewing angle. Jiao *et al*. [10] proposed a corrugated electrode structure which can achieve lower operation voltage (<10 V_{rms}) and higher transmittance (~85.6%). Even though the prior proposed structures successfully lower the operation voltage and achieve high transmittances, the fabrication of the BPLC becomes more complex with the aforementioned structures, leading to the increasing of the fabrication cost and the difficulties of massive production.

As a result, to achieve high transmittance without changing the structure of BPLC, new BPLC pixel circuit enlarging the operation pixel voltage is proposed. The range of the operation pixel voltage is increased to -20 V ~ 20 V from the 0 V ~ 15 V which is generated directly from the data driver IC. Simulation results illustrate that the error rates of the stored voltage are all below 5%, demonstrating that the feasibility of the proposed BPLC pixel circuit and the circuit can be applied to BPLC display applications.

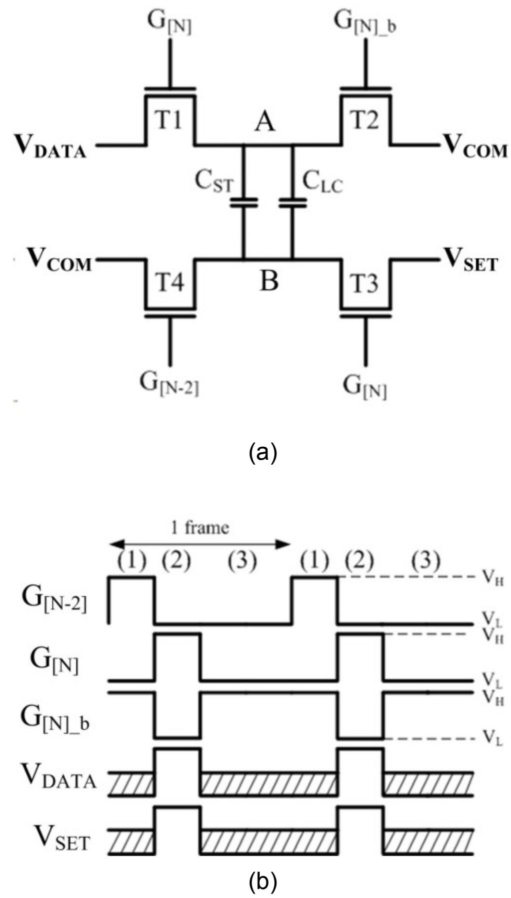


Figure. 1. Proposed a-IGZO TFT BPLC pixel circuit. (a) Schematic diagram and (b) corresponding operation waveforms.

2. Circuit Schematic and Operation

Figure. 1(a) shows the equivalent circuit of the proposed circuit. The circuit is composed of four a-IGZO TFTs and two capacitors. C_{ST} denotes as the storage capacitor for memorizing the data voltage, and C_{LC} denotes as the equivalent capacitor of BPLC. T1, which is controlled by the $G_{[N]}$ signal, is utilized to control the charging of the data voltage. T2 is used to charge node A to V_{COM} for holding the voltage stored in node B. T3 and T4 control the voltage of node B by charging node B to V_{SET} and V_{COM}, respectively. Figure. 1(b) shows the corresponding timing diagram of the proposed circuit. $G_{[N]}$, $G_{[N-2]}$, and $G_{[N]\_b}$ are the scan signals provided by gate driver circuit, and the V_{DATA} and V_{SET} are the data signal provided by data driver ICs.

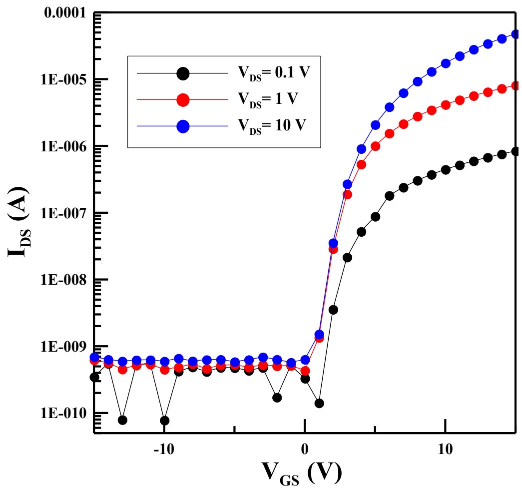


Figure. 2. Transfer characteristics of a-IGZO TFT with W/L=40 μm/ 10 μm

Notably, V_{SET} signal, which has three voltage levels, will be modified based on the desired operation pixel voltage. The circuit operation can be divided into three periods as follows:

Period (1): In this period, $G_{[N-2]}$ and $G_{[N]\_b}$ are at V_H to turn on T2 and T4, respectively. The voltage of node A is kept at V_{COM}, while node B is charged from the voltage in the previous frame to V_{COM} to reset the voltage of node B.

Period (2): When $G_{[N]}$ is changed from V_L to V_H, T1 is turned on and the V_{DATA} is transmitted to node A. At the same time, T3 is turned on to charge node B to V_{SET} according to the desired operation voltage.

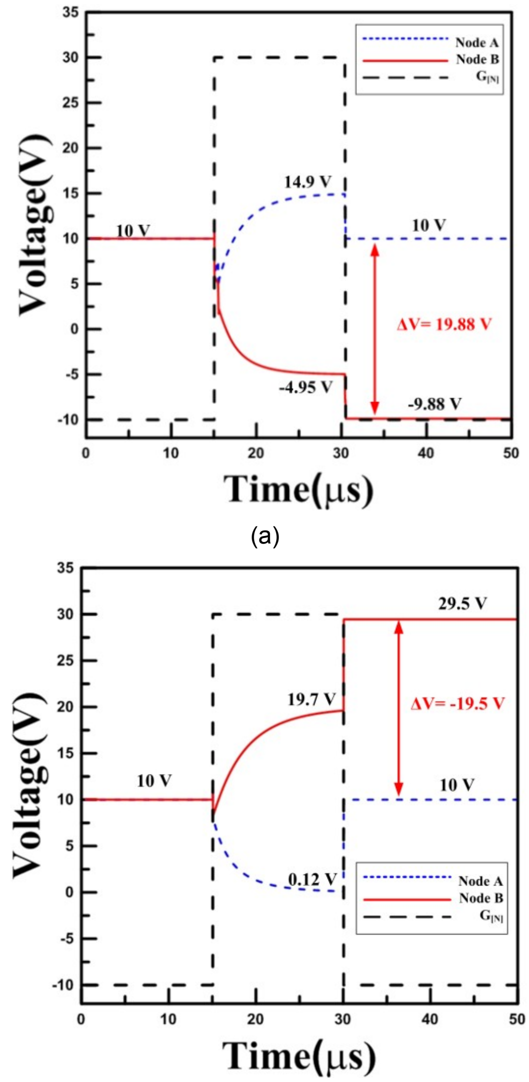
Period (3): When $G_{[N]}$ is changed to V_L and $G_{[N]\_b}$ is changed from V_L to V_H, T1 and T3 are turned off and T2 is turned on. Thus, the voltage of node A is settled to V_{COM} and the voltage of node B would be changed to a V_{SET} - V_{DATA} + V_{COM} by capacitive coupling. Therefore, the operation voltage can be expressed as follows:

$$\begin{aligned} V_{operation} &= V_A - V_B \\ &= V_{COM} - V_{SET} + V_{DATA} - V_{COM} \\ &= V_{DATA} - V_{SET} \end{aligned}$$

As a result, the range of the operation voltage can be modified based on the voltage of V_{SET} and the transmittance could be improved with the enlarged operation pixel voltage.

3. Results and Discussion

The proposed BPLC pixel circuit is simulated through HSPICE simulator to verify the feasibility of the circuit. The characteristics of a-IGZO TFT is modeled with the Rensselaer Polytechnic Institute (RPI) model (*level* = 62), while the parameters in the model are extracted from the measured a-IGZO TFT as shown in Figure. 2. The field-effect mobility and the threshold voltage of the measured a-IGZO TFT are 15.54 cm^2/V and 1.0375 V, respectively. The on/off-current ratio is about 10^6, and the sub-threshold slope is 0.73. Therefore, the device exhibits enhancement-mode operation. The widths and lengths of all the TFTs used in the proposed circuit are 100 μm and 10 μm, respectively. The capacitances of C_{LC} and C_{ST} are both set to 10 pF based on the measured data from BPLC. The V_{COM} is set to 10 V in the simulation. The voltage swings of $G_{[N]}$ signal is -10 V to 30 V, while the range of V_{DATA}, which is restricted by the specification of data driver IC, is 0 V to 15 V. Notably, considering using a 120 Hz FHD (1920×1080) displays, the pulse width of $G_{[N]}$ signal is 15 μs with a pre-charge method.

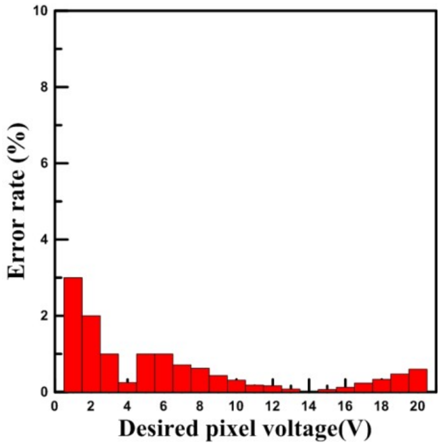


(a)

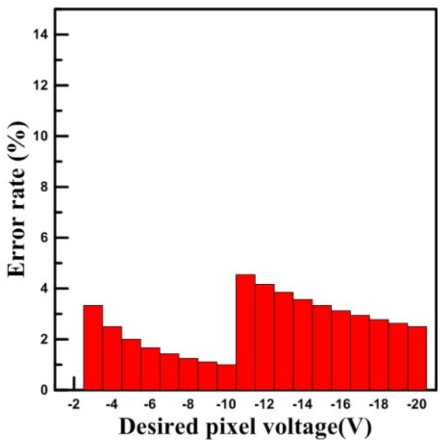
(b)

Figure. 3. Simulated transient waveforms of proposed BPLC pixel circuit (a) Ideal operation pixel voltage = 20 V (b) Ideal operation pixel voltage = -20 V

Figure. 3(a) shows the transient waveforms of the proposed BPLC pixel circuit in positive polarity. While the V_{DATA} is set to 15 V, the V_{SET} is set to -5 V to raise operation pixel voltage to 20 V. As shown in Figure. 3(a), node A and B are charged to 10 V during period (1). In period (2), node A is charged to 14.9 V through T1, while node B is discharge to -4.95 V. In the third period, when node A is discharged to 10 V, node B is simultaneously changed to -9.98 V by capacitive coupling. Therefore, the operation pixel voltage is increased to 19.88 V,



(a)



(b)

Figure. 4. Simulated stored voltage error rates of proposed pixel circuit with different desired operation pixel voltages. (a) Positive polarity and (b) Negative polarity.

and the stored voltage error rate in positive polarity is 0.6 %. Moreover, Figure. 3(b) shows the transient waveforms of the proposed BPLC in negative polarity. In order to decrease the minimum operation pixel voltage to -20 V, V_{SET} is set to 20 V while V_{DATA} is set to 0 V. The voltage of node B reaches 19.7 V in period (2) and node A is discharged to 0.12 V. In period (3), node B is changed to 29.5 V by capacitive coupling as node A is charged to 10 V. Hence, the minimum of the operation pixel voltage is decreased to -19.5 V, and the stored voltage error rate in negative polarity is 2.5 %. As a result, the proposed circuit successfully enlarged the operation voltage to -20 V ~ 20 V.

In order to further verify that the proposed BPLC pixel circuit can generate operation pixel voltage from -20 V to 20 V precisely, Figure .4 shows the corresponding stored voltage error rates with various gray levels. The V_{SET} signal is set to -5 V, 10 V, and 20 V when the ranges of the desired operation voltage are 5 V to 20 V, -10 V to 5 V, and -20 V to -10 V, respectively. As shown in Figure. 4, the error rates of all gray levels are all below 5%, demonstrating that the proposed pixel circuit can be applied to practical panels with BPLCs. Therefore, the simulated results show that proposed BPLC pixel circuit can generate larger pixel operation voltage to improve the transmittance of the BPLC and charge the pixel to the desired voltage precisely.

4. Conclusions

This work presents a new driving pixel circuit with a-IGZO TFT for blue-phase LCDs. The proposed pixel circuit enlarges the operation pixel voltage to increase the transmittance without changing the structure of BPLCs. Simulation results indicate that the proposed circuit successfully increase the range of the operation pixel voltage and the stored operation pixel voltage errors are all below 5%, ensuring that the proposed pixel circuit is suitable for display applications with blue phase liquid crystals

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6. References

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